(54) SOURCE CLOCK REPRODUCING DEVICE, DATA TRANSMISSION EQUIPMENT, DATA RECEPTION EQUIPMENT AND DATA TRANSMISSION SYSTEM

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a stable reproduced clock by reproducing a cycle while using a correction time stamp and a count value outputted from a counter, and reproducing a source clock while using the reproduced cycle.

SOLUTION: Data transmission equipment 10 transmits a transmission time stamp S15 as the differential information of a count value S13 provided by counting up a mesh clock S11 and a cycle TS 14 provided by dividing the frequency of a source clock S12 through a transmission line 15. A time stamp correcting means 22 at data reception equipment 20 corrects the received transmission time stamp S15 and outputs a corrected time stamp S22. A four-bit counter 11 counts up the mesh clock S11 and outputs the count value S13. A comparator 23 reproduces the cycle while using the corrected time stamp S22 a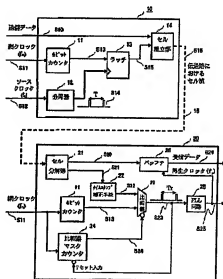nd count value S13 and outputs a reproduced cycle TrS22. A PLL circuit 25 reproduces the source clock S12 while using the reproduced cycle TrS22 and outputs a reproduced clock S25.

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CLAIMS

[Claim(s)]
[Claim 1]Source clock playback equipment comprising:
It generates at the transmitting side which becomes by difference information with a cycle produced
by carrying out dividing of counted value and a source clock which are produced by counting up a
network clock, A time stamp compensation means which receives a time stamp transmitted via a
transmission line, amends the received time stamp concerned, and outputs an amendment time
stamp.
A counter which counts up the above-mentioned network clock and outputs counted value.
A comparator which reproduces the above-mentioned cycle using an amendment time stamp
outputted from the above-mentioned time stamp compensation means, and counted value outputted
from the above-mentioned counter, and outputs a regeneration period.
A PLL circuit which reproduces the above-mentioned source clock using a regeneration period
outputted from the above-mentioned comparator, and outputs a reproduction clock.

[Claim 2]The source clock playback equipment comprising according to claim 1:
A difference calculation circuit which a time stamp compensation means which outputs the above-
mentioned amendment time stamp calculates difference of two time stamps received at intervals of
a constant period among two or more above-mentioned time stamps received one by one, and
outputs the calculation difference value concerned.
A default output means to output a default difference value set up beforehand.
A selector which chooses default either a calculation difference value outputted from the above-
mentioned difference calculation circuit or a difference value outputted from the above-mentioned
default output means, and is outputted as a difference value.
An adding machine which adds a difference value outputted to the above-mentioned amendment
time stamp outputted last time from the above-mentioned selector, generates a new amendment
time stamp recursively and outputs it.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Source clock playback equipment in which this invention reproduces the
source clock frequency of the transmitting side by a receiver, About the data source, a data
receiver, and a data transmission system. For example, the source clock in the data source is
transmitted with a time stamp, and it is related with the source clock playback equipment which
reproduces a source clock from the time stamp with a data receiver, and the data transmission
system using the source clock playback equipment.
[0002]
[Description of the Prior Art]In recent years, the demand to the improvement in the speed to a
network and multimedia-izing increases, and introduction of ATM (Asynchronous Transfer Mode:
Asynchronous Transfer Mode) art is advanced. However, on the other hand, there is STM circuit
service of existing, such as voice communication and a teleconference, and it is necessary with the
spread of ATM networks to accommodate these circuit services to an ATM network. In order to
realize said existing STM circuit service via an ATM network, the art, i.e., source clock reproduction
art, of synchronizing the clock of a circuit by the transmitting side and a receiver is needed.
[0003]As conventional source clock reproduction art, there is a clock reproduction circuit indicated
by JP,8-8918,A, for example. Drawing 18 is a block diagram showing the composition of the
conventional clock reproduction circuit. Operation is explained using drawing 18.
[0004]In the SAR (Segmentation And Reassembly sublayer) header separation part 1, reception of
the cell which is transmitted data transmitted by the ATM transmission system S1 will separate the
SAR header S2. The SAR header S2 separated by the SAR header separation part 1 is constituted
from sequence number protection which protects a sequence number, delta-frequency minute
information, and a sequence number and delta-frequency minute information by the regular format.
[0005]A sequence number is a number series added to a chronological order of a cell in the
transmitting side. The sequence number S3 and delta-frequency minute information S4 are detected
from the SAR header S2 separated by the SAR header separation part 1 by the sequence number
delta-frequency minute information primary detecting element 2. The detected sequence number S3
is supervised by the sequence number Monitoring Department 3, and cell abolition is detected by
the discontinuity of the sequence number S3. And the existence of cell abolition is outputted as the
sequence number monitored result signal S5 from the sequence number Monitoring Department 3.
Management of received delta-frequency minute information S4 is performed by the delta-
frequency part information management forecast processing part 4 with the sequence number
monitored result signal S5.
[0006]When it is usual [which cell abolition or cell delay does not generate] here, With the delta-
frequency part information management signal S6 outputted from the delta-frequency part
information management forecast processing part 4. Received delta-frequency minute information

S4 is recorded instead of the oldest delta–frequency minute information currently recorded on the memory 5, and the delta–frequency minute information of M cycle eye and the delta–frequency minute information of a periodic (M–1) eye are recorded on the memory 5.

[0007]When abandonment of the cell which carried out multiplex [of the delta–frequency minute information of M cycle eye] occurs, the sequence number monitored result signal S5 which detected generating of cell abolition is outputted from the sequence number Monitoring Department 3 to the delta–frequency part information management forecast processing part 4. Then, the predicted value of the delta–frequency minute information of M cycle eye is calculated by data processing using delta–frequency minute information S4 of N cycle eye received correctly before M cycle eye currently recorded on the memory 5 by the delta–frequency part information management forecast processing part 4, The calculated delta–frequency minute information predicted value S7 is outputted to the clock reproduction part 6. And source clock S9 is reproduced using the delta–frequency minute information predicted value S7 in the clock reproduction part 6.

[0008]As mentioned above, according to the conventional clock reproduction circuit, even when cell abolition occurs in an ATM transmission system, influencing of influence in reproduction of the source clock by this cell abolition can be controlled, it is stabilized and a source clock can be reproduced.

[0009]
[Problem(s) to be Solved by the Invention]However, the conventional clock reproduction circuit had the problem that the reproduction clock of a receiver was confused at the time of initial starting of a device provided with the clock reproduction circuit. That is, the conventional clock reproduction circuit reproduces a clock using the delta–frequency minute information memorized at the time of normal [above–mentioned], when the delta–frequency minute information received when [normal] cell abolition or cell delay did not occur is memorized and cell abolition, cell delay, etc. occur. Therefore, since it is in the state before delta–frequency minute information is memorized by the receiver at the time of initial starting, a reproduction clock is confused.

[0010]The problem that a jitter certainly occurred was among the reproduction clocks reproduced by a receiver. That is, in an ATM transmission system, since the delta–frequency minute information used when reproducing a clock is approximated in digital one at the transmitting side, it cannot coincide a reproduction clock with the clock of the transmitting side thoroughly.

[0011]It was made in order to solve the above problems, and this invention is what kind of state (at the time of normal.). At the time of initial starting, at the time of a fault occurrence at the time of cell abolition generating at the time of reset At the time of inaccurate time stamp reception. Disorder of a reproduction clock can be suppressed also in the time of cell delay, etc., and it aims at obtaining the source clock playback equipment, the data source, data receiver, and data transmission system which can reduce the jitter of a reproduction clock.

[0012]
[Means for Solving the Problem]Source clock playback equipment of this invention is characterized by comprising:
It generates at the transmitting side which becomes by difference information with a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock, A time stamp compensation means which receives a time stamp transmitted via a transmission line, amends the received time stamp concerned, and outputs an amendment time stamp.
A counter which counts up the above–mentioned network clock and outputs counted value.
A comparator which reproduces the above–mentioned cycle using an amendment time stamp outputted from the above–mentioned time stamp compensation means, and counted value outputted from the above–mentioned counter, and outputs a regeneration period.
A PLL circuit which reproduces the above–mentioned source clock using a regeneration period outputted from the above–mentioned comparator, and outputs a reproduction clock.

[0013]Source clock playback equipment concerning the next invention, A difference calculation circuit which calculates difference of two time stamps received at intervals of a constant period among two or more above-mentioned time stamps received one by one to a time stamp compensation means which outputs the above-mentioned amendment time stamp, and outputs the calculation difference value concerned to it, A default output means to output a default difference value set up beforehand, A selector which chooses default either a calculation difference value outputted from the above-mentioned difference calculation circuit or a difference value outputted from the above-mentioned default output means, and is outputted as a difference value, A difference value outputted to the above-mentioned amendment time stamp outputted last time from the above-mentioned selector is added, and it has an adding machine which generates a new amendment time stamp recursively and outputs it.

[0014]Source clock playback equipment concerning the next invention, It has a detection means to attain to the above-mentioned time stamp compensation means at the time of reset, or to output a detecting signal to the above-mentioned selector at the time of a fault occurrence in the above-mentioned transmission line, and the above-mentioned selector is constituted so that the above-mentioned default difference value may be chosen based on a detecting signal outputted from the above-mentioned detection means.

[0015]Source clock playback equipment concerning the next invention, It is judged whether a calculation difference value outputted to the above-mentioned time stamp compensation means from the above-mentioned difference calculation circuit is a value of a predetermined permission setting range, When it is values other than the above-mentioned predetermined permission setting range, it has a difference judging means which outputs an unjust detecting signal to the above-mentioned selector, and the above-mentioned selector is constituted so that the above-mentioned default difference value may be chosen based on an unjust detecting signal outputted from the above-mentioned difference judging means.

[0016]Source clock playback equipment concerning the next invention, A difference calculation circuit which calculates difference of two time stamps received at intervals of a constant period among two or more above-mentioned time stamps received one by one to a time stamp compensation means which outputs the above-mentioned amendment time stamp, and outputs the calculation difference value concerned to it, A register which memorizes a calculation difference value outputted from the above-mentioned difference calculation circuit, The 1st adding machine that adds two or more calculation difference values including a calculation difference value memorized by the above-mentioned register, and outputs the total difference value, Add the total difference value outputted to the above-mentioned amendment time stamp outputted last time from the 1st adding machine of the above, have the 2nd adding machine that generates a new amendment time stamp recursively and outputs it, and the above-mentioned counter considers the above-mentioned network clock as an input, It has a clock generating means which generates a clock corresponding to the number of calculation difference values added with the 1st adding machine of the above, and it is constituted so that it may count up with a clock generated by the above-mentioned clock generating means and counted value may be outputted.

[0017]Source clock playback equipment concerning the next invention once accumulates a time stamp received [above-mentioned], and is provided with a time stamp buffer which outputs the time stamp concerned to the above-mentioned time stamp compensation means according to a reproduction clock outputted from the above-mentioned PLL circuit.

[0018]Further again the data source concerning the next invention, A transmitting time stamp creating means which generates a time stamp which becomes by difference information with a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock, When assembling two or more cells and transmitting using two or more transmission data and a time stamp generated by the above-mentioned transmitting time stamp

creating means, it has a cell assembly section which maps the same time stamp information that constitutes the above-mentioned time stamp in two or more cells.

[0019] Further again a data receiver concerning the next invention, A cell containing a time stamp which becomes by difference information with a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock, and transmission data is received via a transmission line, A cell decomposition part which decomposes the cell concerned and outputs a time stamp and transmission data, The above-mentioned time stamp information is compensated with reference to either of two or more same time stamp information that constitutes a time stamp outputted from the above-mentioned cell decomposition part, A time stamp compensation means which amends the time stamp concerned and outputs an amendment time stamp, A counter which counts up the above-mentioned network clock and outputs counted value, A comparator which reproduces the above-mentioned cycle using an amendment time stamp outputted from the above-mentioned time stamp compensation means, and counted value outputted from the above-mentioned counter, and outputs a regeneration period, A PLL circuit which reproduces the above-mentioned source clock using a regeneration period outputted from the above-mentioned comparator, and outputs a reproduction clock, Transmission data outputted from the above-mentioned cell decomposition part is once stored, and it has a buffer which outputs the transmission data concerned according to a reproduction clock outputted from the above-mentioned PLL circuit.

[0020] Further again a data transmission system concerning the next invention, A transmitting time stamp creating means which generates a time stamp which becomes by difference information of a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock to the data source, When assembling a cell and transmitting using transmission data and a time stamp generated by the above-mentioned transmitting time stamp creating means, It has a cell assembly section that maps the same time stamp information that constitutes the above-mentioned time stamp in two or more cells, A cell decomposition part which is assembled by the above-mentioned cell assembly section by data receiver, decomposes into it a cell transmitted via a transmission line, and outputs a time stamp and transmission data to it, The above-mentioned time stamp information is compensated with reference to either of two or more same time stamp information that constitutes a time stamp outputted from the above-mentioned cell decomposition part, A time stamp compensation means which amends the time stamp concerned and outputs an amendment time stamp, A comparator which reproduces the above-mentioned cycle using a counter which counts up the above-mentioned network clock and outputs counted value, and an amendment time stamp outputted from the above-mentioned time stamp compensation means and counted value outputted from the above-mentioned counter, and outputs a regeneration period, A PLL circuit which reproduces the above-mentioned source clock using a regeneration period outputted from the above-mentioned comparator, and outputs a reproduction clock, Transmission data outputted from the above-mentioned cell decomposition part is once stored, and it has a buffer which outputs the transmission data concerned according to a reproduction clock outputted from the above-mentioned PLL circuit.

[0021]
[Embodiment of the Invention] Below embodiment 1. describes an embodiment of the invention using a drawing. In an embodiment, a transmitting time stamp and the time stamp received are explained for the time stamp transmitted, and send data and the transmission data received are explained for a receiving time stamp and the transmission data transmitted as received data.

[0022] Drawing 1 is a block diagram showing the composition of the data transmission system concerning the 1 embodiment of this invention. In drawing 1, 10 is the data source which performs data communications in an ATM network, and 20 is a data receiver.

[0023] 11 is counted up with the network clock S11, it is a counter which outputs the counted value S13, and four bit counters are used for it here. 12 carries out dividing of the source clock S12, is a

counting-down circuit which generates a predetermined periodical pulse, and outputs periodic T S14 as a periodical pulse here.

[0024]13 latches the counted value S13 outputted from the four above-mentioned bit counter 11 every cycle T S14 of the above-mentioned periodical pulse generated with the above-mentioned counting-down circuit 12 (maintenance), He is the latch who outputs the transmitting time stamp S15 which is the difference information of periodic TS14 produced by carrying out dividing of the above-mentioned network clock S11 and the above-mentioned source clock S12. In this embodiment, a transmitting time stamp creating means comprises the four above-mentioned bit counter 11, the counting-down circuit 12, and the latch 13.

[0025]14 is a cell assembly section which assembles the cell S16 and transmits using the send data S10 and the transmitting time stamp S15 outputted by the above-mentioned latch 13. 15 is a transmission line which transmits the cell S16 assembled by the above-mentioned cell assembly section 14.

[0026]21 is a cell decomposition part which decomposes the cell S16 transmitted from the above-mentioned data source 10 via the above-mentioned transmission line 15, and outputs the received data S20 and the receiving time stamp S21. 22 is a time stamp compensation means which calculates the difference of the two receiving time stamps S21 which continue among the receiving time stamps S21 outputted one by one from the above-mentioned cell decomposition part 21, and amends and outputs the amendment time stamp S22 using the difference value.

[0027]While the enable signal S24 outputted from the comparator mask counter 24 which 23 mentions later is asserted, Coincidence detection of the counter value S13 outputted from the four bit counters 11 of the data receiver 20 and the amendment time stamp S22 outputted from the above-mentioned time stamp compensation means 22 is compared and carried out, It is a comparator which reproduces periodic T S14 outputted from the above-mentioned counting-down circuit 12, and outputs regeneration period Tr S23.

[0028]It is a comparator mask counter which makes operation of the above-mentioned comparator 23 fixed time invalidity, if 24 is counted up with the network clock S11 and a predetermined threshold is exceeded, it will assert the enable signal S24, and if regeneration period Tr S23 is outputted from the above-mentioned comparator 23, it will reset a count.

[0029]25 is a PLL circuit (PhaseLock Loop circuit) which reproduces a clock and outputs the reproduction clock S25 by a phase feedback loop using regeneration period Tr S23 outputted from the above-mentioned comparator 23. 26 is a buffer which outputs the received data S26 according to the reproduction clock S25 which once accumulates the received data S20 outputted from the above-mentioned cell decomposition part 21, and is outputted from above-mentioned PLL circuit 25.

[0030]Next, operation is explained. Although the case where the source clock S12 is the 1.544 MHz is explained as an example for simplification, the range of source clock frequency is not limited. Although the basic transmission rates in an ATM network are 155.52Mbps or 622.08Mbps, according to TTC standard JT-I363, when frequency of fn and the source clock S12 is set to fs, there is restriction of 1<fn/fs<=2 about the frequency of the network clock S11.

[0031]For this reason, the frequency of the network clock S11 sets 155.52 MHz to 2.43 MHz which 2 squared -6 here. Although the case where bit width of a time stamp is set to 4 is explained based on TTC standard JT-I363, using the four bit counters 11 as a counter, it cannot be overemphasized that it may be the bit width of the other counter and a time stamp.

[0032]In the data source 10, the counted value S13 unconditionally counted up with the network clock S11 is first outputted from the four bit counters 11. Periodic T S14 produced from the counting-down circuit 12 by carrying out dividing of the source clock S12 on the other hand is outputted. In this embodiment, this periodic T S14 is a data forwarding period for eight cells.

[0033]Then, the counted value S13 which is outputted from the above-mentioned counting-down circuit 12 by the latch 13 and which is outputted from the four above-mentioned bit counter 11

every cycle T S14 is latched, and it is outputted to the cell assembly section 14 as the transmitting time stamp S15.

[0034]In this embodiment, the value of a transmitting time stamp is the remainder which added the value of the last transmitting time stamp to the periodicity of the cycle T by network clock conversion, and was divided by 16. As mentioned above, periodic T S14 is equivalent to the sending-out period for eigt cells of the cell S16, and is a part for 3008 clocks of source clock frequency, i.e., 1.948 ms. The value will be set to 4733 or 4334 if network clock conversion of this is carried out. The value of the last transmitting time stamp is added to this value, and the remainder divided by 16 serves as a value of this transmitting time stamp.

[0035]If the transmitting time stamp S15 is outputted to the cell assembly section 14 from the above-mentioned latch 13, in the cell assembly section 14, the cell S16 will be assembled using the transmission data S10 and the above-mentioned transmitting time stamp S15, and the cell S16 will be sent out to the data receiver 20 via the transmission line 15.

[0036]Drawing 2 is a key map showing the composition of the cell of the 53-byte length by the AAL (ATM adaptation layer) type 1. 5 bytes of ATM header in which D1 stores the header information of ATM transmission in drawing 2, 1 byte of SAR-PDU header in which D2 stores the header information of transmitted data (Segmentation And Reassembly-Protocol Data Unit header), The SAR-PDU pay load in which D3 stores send data, the CSI bit in which D4 stores a time stamp (Convergence Sublayer Indication bit), SC field (Sequence field) where D5 stores a sequence number, the CRC field (Cyric Redundancy Check field) which uses D6 for a Cyclic Redundancy Check, and D7 are even parity used for a parity check.

[0037]The send data S10 is mapped by the SAR-PDU pay load D3, the transmitting time stamp S15 is mapped by CSI bit D4, respectively, and the cell S16 is assembled by the cell assembly section 14.

[0038]Drawing 3 is a key map showing the example which seems to map a transmitting time stamp in the cell S16 in the cell assembly section 14. In the case of drawing 3, the 4-bit transmitting time stamp S15 is divided into every 1 bit of transmitting time stamp information, and the SC field D5 is mapped by CSI bit D4 of the cell whose number is odd among the eight cells S16.

[0039]Next, the data receiver 20 is explained. First, the cell S16 transmitted from the data source 10 is decomposed by the cell decomposition part 21, the received data S20 are outputted to the buffer 26, and the receiving time stamp S21 is outputted to the time stamp compensation means 22.

[0040]In [if the above-mentioned receiving time stamp S21 is outputted to the time stamp compensation means 22] the time stamp compensation means 22, The difference of the last above-mentioned receiving time stamp S21 and this receiving time stamp S21 is calculated among the receiving time stamps S21 inputted one by one, and the amendment time stamp S22 amended using the difference value is outputted to the comparator 34. Detailed operation of the time stamp compensation means 22 is mentioned later.

[0041]On the other hand, from the four bit counters 11, the counted value S13 unconditionally counted up with the network clock S11 is outputted to the comparator 23. If it counts up with the network clock S11 and a threshold is exceeded until it exceeds a threshold at the comparator mask counter 24 simultaneously with this, the enable signal S24 will be asserted.

[0042]While the above-mentioned enable signal S24 is asserted, by the comparator 23. Coincidence detection of the counted value S13 outputted from the four above-mentioned bit counter 11 and the amendment time stamp S22 outputted from the above-mentioned time stamp compensation means 22 is performed, periodic T S14 outputted from the above-mentioned counting-down circuit 12 is reproduced from the result, and regeneration period TrS23 is outputted.

[0043]Here, a value a little smaller than the minimum which periodic T S14 can take is used for the threshold of the above-mentioned comparator mask counter 24. For example, when the transfer characteristic of the source clock S12 with a frequency of 1.544 MHz sets to **100 ppm, periodic T

S14 is a part for 4733 to 4735 clock in network clock S11 conversion. Therefore, what is necessary is just to choose about 4730 as the above-mentioned threshold. By doing in this way, the comparator 23 can obtain regeneration period Tr S23.

[0044]And if regeneration period TrS23 is outputted from the above-mentioned comparator 23, the comparator mask counter 24 will be reset. If regeneration period Tr S23 outputted from the above-mentioned comparator 23 is inputted into PLL circuit 25, a clock will be reproduced by the phase feedback loop in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 will be outputted. Then, according to the reproduction clock S25, the received data S26 are outputted from the above-mentioned received buffer 26. Thus, periodic T S14 of the data source 10 can be reproduced as regeneration period Tr S23 with the data receiver 20, and received data can be read.

[0045]Next, the above-mentioned time stamp compensation means 22 which is a main part of this embodiment is explained in detail. Drawing 4 is a block diagram showing the composition of the above-mentioned time stamp compensation means 22. In drawing 4, 31 is the default difference value S30 set up beforehand a default output means to output, and here, The value "+14" generated most frequently as a difference value of two receiving time stamps which continue among the receiving time stamps S21 outputted one by one from the cell decomposition part 21 is outputted as a default difference value. 32 is a difference calculation circuit which calculates the difference of the two receiving time stamps S21 which continue among the receiving time stamps S21 outputted one by one from the cell decomposition part 21, and outputs the calculation difference value S31.

[0046]33a is a detection means to output a detecting signal, and when the reset signal S32 from the system monitoring part which is not illustrated is detected here and the reset signal S32 is detected, it is a reset signal detection means which outputs the reset detecting signal S33. For example, the above-mentioned system monitoring part 33a outputs the above-mentioned reset signal S32 at the time of the reset at the time of reset of the device by a user, etc. at the time of the restoration from a line disruption or device failure generating at the time of initial starting of a system.

[0047]34 chooses default either the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 or the difference value outputted from the above-mentioned default output means 31 S30, Based on the reset detecting signal S33 which is a selector outputted as the difference value S34, and is outputted from the above-mentioned reset signal detection means 33a, At the time of reset, the default difference value S30 outputted from the above-mentioned default output means 31 is chosen, and when it is not at the reset time, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen. 35 is an adding machine which adds the difference value S34 outputted to the amendment time stamp S22 outputted last time from the above-mentioned selector 34, generates the new amendment time stamp S22 recursively, and outputs it.

[0048]Operation of the time stamp compensation means 22 is explained. Drawing 5 is a key map showing the concept of operation at the time of normal of the time stamp compensation means 22 by the composition of drawing 4. The receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 is inputted into the difference calculation circuit 32 of the time stamp compensation means 22.

[0049]Then, the default difference value S30 is outputted to the selector 34 from the default output means 31. On the other hand, from the difference calculation circuit 12, the difference of the two receiving time stamps S21 which continue among the receiving time stamps S21 outputted one by one from the above-mentioned cell decomposition part 21 is calculated, and the calculation difference value S31 is outputted to the selector 34.

[0050]For example, when the receiving time stamp S21 "14" is inputted into the difference calculation circuit 32 and the receiving time stamp S21 "12" is inputted last time this time, the calculation difference value S31 is set to "12−14=+14."

[0051]Since the reset signal detection means 33a to the reset detecting signal S33 is not outputted at the time (when it is not at the reset time) of normal, in the selector 34, the calculation difference value S31 outputted from the difference calculation circuit 32 is chosen, and the difference value S34 is outputted to the adding machine 35.

[0052]Then, with the adding machine 35, the difference value S34 outputted from the above-mentioned selector 34 is added to the amendment time stamp S22 outputted last time, and is outputted as this amendment time stamp S22. For example, the calculation difference value S31 outputted from the above-mentioned selector 34 is "+14", and when the amendment time stamp S22 outputted last time is "8", this amendment time stamp S22 is set to "8+(+14) =6."

[0053]Thus, at the time of normal, an amendment time stamp is generated using the calculation difference value S31 calculated from the receiving time stamp S21, and it is outputted to the comparator 23.

[0054]Next, the operation at the time of reset is explained. Drawing 6 is a key map showing the concept of operation at the time of reset of the time stamp compensation means 22 by the composition of drawing 4. In drawing 6, S21a is the receiving time stamp received at the time of reset.

[0055]At the time of reset, while the received receiving time stamp S21a is inputted, the reset signal S32 is detected and the reset detecting signal S33 is outputted to the selector 34 by the reset signal detection means 33a.

[0056]On the other hand, if the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 is inputted into the difference calculation circuit 32 of the time stamp compensation means 22 like the time of normal at the time of reset, The default difference value S30 "+14" is outputted to the selector 34 from the default output means 31, and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 12.

[0057]Then, in the selector 34, the default difference value S30 "+14" outputted from the above-mentioned default output means 31 based on the reset detecting signal S33 outputted from the reset signal detection means 33a is chosen, and this is outputted as the difference value S34.

[0058]And with the adding machine 35, the difference value S34 outputted from the above-mentioned selector 34 is added to the amendment time stamp S22 outputted last time, and is outputted to the comparator 23 as this amendment time stamp S22. Thus, since the default difference value S30 outputted by the selector 34 from the default output means 31 is chosen at the time of reset, the receiving time stamp S21a at the time of reset is not reflected in the amendment time stamp S22.

[0059]The receiving time stamp S21a received at the time of reset has an unstable state of a system, and the timing of reception is changed. It is in the state before receiving the receiving time stamp S21 especially at the time of initial starting of a system. Therefore, by not reflecting the receiving time stamp S21a at the time of reset in the amendment time stamp S22, since the calculation difference value S31 is correctly incalculable, The time stamp compensation means 22 can generate the amendment time stamp S22 at the time of reset, and the data receiver 20 can reproduce stable regeneration period Tr S23.

[0060]Then, if time passes and a system becomes normal, a reset signal will no longer be detected by the reset signal detection means 33a. Then, the reset detecting signal S33 is no longer outputted from the reset signal detection means 33a, and the calculation difference value S31 outputted from the difference calculation circuit 32 comes to be chosen by the selector 34 like the operation at the above-mentioned time of normal.

[0061]According to this embodiment, the stable reproduction clock can be obtained as mentioned above by amending a receiving time stamp using the calculation difference value calculated from two continuous receiving time stamps, and generating an amendment time stamp with a data receiver.

[0062]A data receiver generates an amendment time stamp using the calculation difference value calculated from two receiving time stamps which continue at the time of normal, By generating an

amendment time stamp using the default difference value beforehand set up at the time of reset, and reproducing the source clock of the transmitting side using the amendment time stamp, the time of the reset which it not only can obtain the reproduction clock stable at the time of normal, but includes the time of initial starting of a system — being also alike — big disturbance cannot be given and a reproduction clock can be obtained.

[0063]Although this embodiment explained the case where a calculation difference value was calculated from two continuous receiving time stamps, it is not limited to this. The calculation difference value is just a difference value of the receiving time stamp of a constant period interval, for example, may be a difference value of the receiving time stamp in every other one. In this case, although time until a reproduction clock is stabilized increases somewhat, the jitter of a reproduction clock is mitigable.

[0064]Although the embodiment of the embodiment 2. above-mentioned can form the reset signal detection means 33a in the time stamp compensation means 22 and the reproduction clock stable also at the time of reset can be obtained, Next, the embodiment which can obtain the reproduction clock stable when the obstacle in a transmission line occurred is shown.

[0065]Drawing 7 is a block diagram showing the composition of the time stamp compensation means 22 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. 13b is a detection means to output a detecting signal to the selector 34, and when the sequence number S35 of the cell stored in the SC field D5 shown in drawing 2 here is supervised, an obstacle is detected and an obstacle is detected, it is a fault detection means which outputs the failure detection signal S33 to the selector 34. Here, the sequence number S35 is inputted from the cell decomposition part 21 shown in drawing 1. An obstacle is an obstacle in a transmission line detectable from the sequence number S35, and are obstacles that the cell erroneous insertion which the cell loss (cell abolition) to which a cell does not reach a receiver, and an unnecessary cell reach, and an attainment order of a cell are confused, such as a sequence error.

[0066]Based on the failure detection signal S33 outputted from the above-mentioned fault detection means 33b, the selector 34, The default difference value S30 outputted from the above-mentioned default output means 31 is chosen, at the time of a fault occurrence, when it is not at the reset time, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and it outputs the difference value S34.

[0067]Operation is explained. Drawing 8 is a key map showing the concept of operation at the time of the fault occurrence of the time stamp compensation means 22 by the composition of drawing 7. In drawing 8, S21b is the time stamp lost at the time of a fault occurrence, and shows that a time stamp did not reach to a data receiver.

[0068]At the time of normal, an obstacle is not detected and the failure detection signal S33 is not outputted to the selector 34 by the obstacle inspection means 33b (when an obstacle does not occur). Therefore, after the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 was inputted into the difference calculation circuit 32 of the time stamp compensation means 22, If the default difference value S30 is outputted to the selector 34 from the default output means 31 and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 32, In the selector 34, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and this is outputted to the adding machine 35 as the difference value S34.

[0069]That is, while the receiving time stamp S21 is normally transmitted with "3, 1, 14", the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen by the selector 34, and "+13, +14" are outputted in order to the adding machine 35 as the difference value S34.

[0070]On the other hand, at the time of a fault occurrence, an obstacle is detected from the sequence number S35, and the failure detection signal S33 is outputted to the selector 34 by the

obstacle inspection means 33b. Then, after the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 was inputted into the difference calculation circuit 32 of the time stamp compensation means 22, If the default difference value S30 is outputted to the selector 34 from the default output means 31 and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 32, The default difference value S30 outputted from the above-mentioned default output means 31 is chosen by the selector 34, and this is outputted to the adding machine 35 as the difference value S34.

[0071]That is, when a receiving time stamp does not reach like the lost time stamp S21b, the default difference value S30 "+14" outputted from the above-mentioned default output means 31 is chosen by the selector 34, and "+14" is outputted to the adding machine 35 as the difference value S34.

[0072]If the difference value S34 is outputted to the adding machine 35 from the above-mentioned selector 34, like the above-mentioned embodiment, the amendment time stamp S22 will be generated by the adding machine 35, and it will be outputted to the comparator 23. Regeneration period Tr S23 is reproduced using the above-mentioned amendment time stamp S22 by the comparator 23, a clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0073]According to this embodiment, a data receiver generates an amendment time stamp using the calculation difference value calculated from two receiving time stamps which continue at the time of normal as mentioned above, By generating an amendment time stamp using the default difference value beforehand set up at the time of a fault occurrence, and reproducing the source clock of the transmitting side using the amendment time stamp, At the time of a fault occurrence, when an obstacle occurs in a transmission line and a time stamp does not arrive for example, it cannot give big disturbance and it not only can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.

[0074]Although this embodiment explained the case where a calculation difference value was calculated from two continuous receiving time stamps, the calculation difference value should just be a difference value of the receiving time stamp of a constant period interval, and it cannot be overemphasized that it is not what is limited to this.

[0075]Although the reproduction clock stable also at the time of reset and a fault occurrence can be obtained in the embodiment of the embodiment 3. above-mentioned next, the embodiment which can obtain the reproduction clock stable when an inaccurate time stamp was received is shown.

[0076]Drawing 9 is a block diagram showing the composition of the time stamp compensation means 22 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. 33c supervises the calculation difference value S32 outputted from the difference calculation circuit 12, It is a difference judging means which judges whether the calculation difference value S32 is a value of the permission setting range as a difference value of a time stamp, judges with having received the time stamp inaccurate when it is values other than a permission setting range, and outputs the unjust detecting signal S33 to the selector 34. For example, the permission setting range as a time stamp difference value is set as +13~+15.

[0077]Based on the unjust detecting signal S33 outputted from the above-mentioned difference judging means 33c, the selector 34, When values other than the permission setting range as a time stamp difference value occur, the default difference value S30 outputted from the above-mentioned default output means 31 is chosen, when other, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and the difference value S34 is outputted.

[0078]Operation is explained. In the time stamp compensation means 22 by the composition of drawing 9, drawing 10 is a key map showing a concept of operation when values other than the permission setting range as a time stamp difference value occur.

[0079]If the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 is inputted into the difference calculation circuit 32 of the time stamp compensation means 22 like the above-mentioned embodiment, The default difference value S30 is outputted to the selector 34 from the default output means 31, and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 32.

[0080]It can come, simultaneously the calculation difference value S31 from the above-mentioned difference calculation circuit 32 is outputted to the difference judging means 33c. Then, it is judged whether the above-mentioned calculation difference value S31 is a value of the permission setting range as a difference value of a time stamp in the difference judging means 33c.

[0081]As a result, when the above-mentioned calculation difference value S31 is a value in a permission setting range, it is not judged with having received the inaccurate time stamp, and the unjust detecting signal S33 is not outputted from the difference judging means 33c. In this case, in the selector 34, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and this is outputted to the adding machine 35 as the difference value S34. That is, when the difference value of the two continuous receiving time stamps S21 is +13→+15, the above-mentioned calculation difference value S31 is chosen by the selector 34.

[0082]On the other hand, when the above-mentioned calculation difference values S31 are values other than a permission setting range, it judges with having received the inaccurate time stamp, and the unjust detecting signal S33 is outputted to the selector 34 from the above-mentioned difference judging means 33c. Then, in the selector 34, the default difference value S30 outputted from the above-mentioned default output means 31 based on the above-mentioned unjust detecting signal S33 is chosen, and it is outputted to the adding machine 35 as the difference value S34.

[0083]That is, for example, in drawing 10, the last receiving time stamp S21 is "14", and when this receiving time stamp S21 is "9", the calculation difference value S31 is set to "14-9=+11." However, since "+11" is outside the range of a permission setting range (+13→+15), the unjust detecting signal S33 is outputted to the selector 34 from the above-mentioned difference judging means 33c, and the above-mentioned default difference value S30 "+14" is chosen based on the above-mentioned unjust detecting signal S33 in the selector 34.

[0084]If the difference value S34 is outputted to the adding machine 35 from the above-mentioned selector 34, like the above-mentioned embodiment, the amendment time stamp S22 will be generated by the adding machine 35, and it will be outputted to the comparator 23. Regeneration period Tr S23 is reproduced using the above-mentioned amendment time stamp S22 by the comparator 23, a clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0085]As mentioned above, when the calculation difference values calculated from two continuous receiving time stamps are values other than the permission setting range as a time stamp difference value according to this embodiment, By generating an amendment time stamp using the default difference value set up beforehand, and reproducing the source clock of the transmitting side using the amendment time stamp, When values other than the permission setting range as a difference value of a time stamp occur, and an inaccurate time stamp is received for example, it cannot give big disturbance and it not only can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.

[0086]Although this embodiment explained the case where a calculation difference value was calculated from two continuous receiving time stamps, the calculation difference value should just be a difference value of the receiving time stamp of a constant period interval, and it cannot be overemphasized that it is not what is limited to this.

[0087]Although an amendment time stamp is generated from one difference value next, the embodiment of the embodiment 4. above-mentioned extends the number of bits of the counter of a data receiver, makes an operation clock increase, and shows the embodiment which generates an

amendment time stamp from two or more difference values.

[0088]Drawing 11 is a block diagram showing the composition of the time stamp compensation means 22 concerning this embodiment. In drawing 11, identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted.

[0089]36 is a register outputted as the calculation difference value S36 of 1 time ago, when the calculation difference value S31 outputted from the difference calculation circuit 32 is memorized and the following calculation difference value S31 is further outputted from the above-mentioned difference calculation circuit 32.

[0090]37 is the 1st adding machine that adds the calculation difference value S36 before [one] being outputted from the calculation difference value S31 and the above-mentioned register which are outputted from the above-mentioned difference calculation circuit 32, and outputs the total difference value S37. 38 is an adding machine which adds the total difference value S37 outputted to the amendment time stamp S22 outputted last time from the 1st adding machine 37 of the above, generates the new amendment time stamp S22 recursively, and outputs it.

[0091]Drawing 12 is a block diagram showing the composition of the data receiver 20 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. 27 is a clock generating means which generates the clock corresponding to the number of the calculation difference values added with the 1st adding machine of the above by considering the network clock S11 as an input. Here, since two calculation difference values are added with the 1st adding machine of the above, the clock which is twice the network clock is generated.

[0092]28 is the counted value S22 counted up with the clock generated by the above-mentioned clock generating means 27 an extended counter to output, and here, since an operation clock (network clock) doubles by the above-mentioned clock generating means 27, five bit counters which carried out 1 bit extension of the four bit counters are used. In this embodiment, a counter comprises the above-mentioned clock generating means 27 and five above-mentioned bit counter. Like the above-mentioned embodiment, although the time stamp compensation means 22 generates the amendment time stamp S22, it generates the amendment time stamp corresponding to 5 bits here.

[0093]Operation is explained. Drawing 13 is a key map showing the concept of operation of the time stamp compensation means 22 in this case. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. S31 is the calculation difference value outputted from the difference calculation circuit 32, and is outputted in order of a, b, and c. S36 is the last calculation difference value outputted from the register 36 according to the timing to which the above-mentioned calculation difference value S31 is outputted, and d, e, and f are the same as the above-mentioned a, b, and c respectively. S37 is the total difference value outputted from the 1st adding machine 37 of the above.

[0094]First, like the above-mentioned embodiment, if the receiving time stamp S21 is inputted into the difference calculation circuit 32, the calculation difference value S31 will be outputted. In an initial state, the calculation difference value S31a "+14" is memorized by the register 36 as the last calculation difference value S36d "+14."

[0095]And if the following receiving time stamp S21 is inputted into the difference calculation circuit 32, the calculation difference value S31b "+14" will be outputted from the difference calculation circuit 32, and it will be inputted into the 1st adding machine 37. It can come, simultaneously the last calculation difference value S36d "+14" is outputted from the above-mentioned register 36, and it is inputted into the 1st adding machine 37.

[0096]Then, the above-mentioned calculation difference value S31b "+14" and the last above-mentioned calculation difference value S36d "+14" are added with the 1st adding machine 37, and the total difference value S37g "+28" is inputted into the 2nd adding machine 38. In the 2nd adding machine 38, the total difference value S37g "+28" is added to the amendment time stamp "11"

outputted last time, and the new amendment time stamp S22 "7" is outputted.

[0097]By thus, the thing for which the amendment time stamp S22 corresponding to an extension bit is generated from the total difference value S37 adding this calculation difference value S31 and the last calculation difference value S36. Equalizing the error (change) of an amendment time stamp and equalizing the error given to regeneration period Tr S23 can carry out, and the jitter of the reproduction clock S25 can be reduced.

[0098]That is, since a time stamp is approximated in digital one at the transmitting side, disorder arises in a calculation difference value in a receiver. For example, in the calculation difference value S31, only the calculation difference value S31c is set to "+13." For this reason, when not extending the amendment time stamp of a receiver, a gap arises in an amendment time stamp in this portion, it is confused to regeneration period Tr S23 generated using this amendment time stamp, and a jitter arises in the reproduction clock S25.

[0099]On the other hand, in the case where the amendment time stamp of a receiver is extended, "+27" is repeated twice with the total difference value S37. That is, if "+27" is converted into the usual network clock, it is "+13.5" and the error given to regeneration period Tr S23 can be equalized. Therefore, clock reproduction can be carried out using regeneration period Tr S23 equalized, and the jitter of the reproduction clock S25 can be reduced.

[0100]According to this embodiment, 1 bit extension of the four bit counters of a data receiver is carried out as mentioned above, By making an operation clock increase twice and generating the amendment time stamp corresponding to an extension bit from the total difference value adding this calculation difference value and the last calculation difference value, Few amendment time stamps with error (change) are generable, and since the error given to regeneration period Tr S23 can be equalized, the jitter of a reproduction clock is mitigable.

[0101]Although carried out 1 bit extension of the four bit counters, the operation clock was made to increase twice and the case where an amendment time stamp was generated from the total difference value of two difference values was explained by this embodiment, it is not limited to this. k (k is natural number) bit extension carries out N (N is natural number) bit counter, an operation clock is made to increase by m times (m is the k-th power of 2), and it may be made to generate an amendment time stamp from the total difference value of the difference value of 2^k individual.

[0102]In this case, a clock generating means is constituted so that the clock corresponding to the number k of extension bits may be generated, and an extended counter uses a N+k bit counter. A time stamp compensation means is made composition as shown in drawing 14, for example. Drawing 14 is a block diagram showing the composition of the time stamp compensation means in the case of using a N+k bit counter, gives identical codes to a portion the same as that of drawing 11, or considerable, and omits explanation.

[0103]36 is a register group which memorizes the calculation difference value outputted from the difference calculation circuit 32, and comprises a register of 2^{k-1} individual mentioned later. 361 is the 1st register outputted as the calculation difference value S361 of 1 time ago, when the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is memorized and the following calculation difference value S31 is further outputted from the above-mentioned difference calculation circuit 32. 362 is the 2nd register outputted as the calculation difference value S362 of 2 times ago, when the calculation difference value S361 before [one] being outputted from the 1st register of the above is memorized and the following calculation difference value S31 is further outputted from the above-mentioned difference calculation circuit 32. Similarly 363 memorizes the calculation difference value in front of 2^{k-2} time outputted from the 2nd $^{k-2}$ register, When the following calculation difference value S31 is furthermore outputted from the above-mentioned difference calculation circuit 32, it is the 2nd $^{k-1}$ register outputted as the calculation difference value S363 in front of 2^{k-1} time.

[0104]Thus, k bit extension the counter of a data receiver by carrying out, making an operation

clock increase by m times (m is the k-th power of 2), and generating the amendment time stamp corresponding to a N+k bit from the total difference value adding the calculation difference value of k pieces, Computational complexity and the number of registers increase so that several k of the calculation difference value to add is large, but the jitter of a reproduction clock is more mitigable.

[0105]Although the case where a calculation difference value was calculated from two continuous receiving time stamps was explained, the calculation difference value should just be a difference value of the receiving time stamp of a constant period interval, and it cannot be overemphasized that it is not what is limited to this.

[0106]The embodiment of the embodiment 5. above-mentioned shows the embodiment which generates an amendment time stamp according to cell delay fluctuation, although an amendment time stamp is generated according to the timing which a cell reaches to a data receiver next.

[0107]Drawing 15 is a block diagram showing the composition of the data receiver 20 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. The buffer 26 comprises a data buffer which accumulates the received data S20 disassembled and outputted by the cell decomposition part 21, and a time stamp buffer which accumulates the receiving time stamp S21, The above-mentioned received data S20 and the receiving time stamp S21 are once accumulated, and the received data S26 and the receiving time stamp S21 are outputted according to the reproduction clock S25 outputted from PLL circuit 25.

[0108]Operation is explained. The cell transmitted from the data source 10 is decomposed into the received data S20 and the receiving time stamp S21 by the cell decomposition part 21, and the received data S20 and the receiving time stamp S21 which were disassembled [above-mentioned] are accumulated in the buffer 26. At this time, 1 or two or more receiving time stamps S21 are accumulated in the buffer 26 according to the situation of cell delay fluctuation of a transmission line.

[0109]The receiving time stamp S21 accumulated in the above-mentioned buffer 26 is read according to the reproduction clock S25 outputted from PLL circuit 25, and is outputted to the time stamp compensation means 22.

[0110]Henceforth, like the above-mentioned embodiment, the amendment time stamp S22 is outputted to the comparator 23 from the time stamp compensation means 22, and regeneration period Tr S23 is reproduced by the comparator 23. And a clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0111]By once accumulating a receiving time stamp in a buffer, and reading from a buffer according to a reproduction clock according to this embodiment, as mentioned above, A receiving time stamp can be prevented from being influenced by the cell delay fluctuation in a transmission line, and disorder of a reproduction clock can be suppressed.

[0112]When a transmitting time stamp is mapped in a cell by a cell assembly section, a sequence number maps a transmitting time stamp in odd cells (an odd number cell is called hereafter.), but the embodiment of the embodiment 6. above-mentioned. Next, a sequence number maps a transmitting time stamp also in even cells (an even number cell is called hereafter.), and the embodiment with which the loss of a receiving time stamp is compensated is shown.

[0113]Drawing 16 is a key map showing signs that the cell assembly section 14 maps a transmitting time stamp in a cell in this embodiment. Identical codes are given to an above-mentioned embodiment and identical parts, and explanation is omitted. When the cell assembly section 14 assembles a cell and transmits using send data and the transmitting time stamp outputted by the latch 13, it maps the same transmitting time stamp information that constitutes the above-mentioned transmitting time stamp in two or more cells.

[0114]Operation is explained. In the above-mentioned cell assembly section 14, when the 4-bit transmitting time stamp S15 is mapped in eight cells, it maps each 1 bit of transmitting time stamp

information of the 4 above-mentioned bits transmitting time stamp S15 in every two continuous cells (an odd number cell and an even number cell). That is, in drawing 16, after mapping 1 bit of transmitting time stamp information of the transmitting time stamp S15 in the odd number cell C1, 1 bit of the same transmitting time stamp information also as the continuing even number cell C2 is mapped. Similarly, every 1 bit of the respectively same transmitting time stamp information as the odd number cell C3, the even number cell C4 and the odd number cell C5, the even number cell C6 and the odd number cell C7, and the even number cell C8 is mapped.

[0115]When the obstacle 33b in a transmission line detectable from a sequence number, for example, the above-mentioned fault detection means, detects the cell loss of an odd number cell, with reference to the information on the receiving time stamp S21 of an even number cell, the loss of the information on a receiving time stamp is compensated with the data receiver 20.

[0116]And the amendment time stamp created using the information on the receiving time stamp which the account of the upper compensated from the time stamp compensation means 22 is outputted to the comparator 23, and regeneration period Tr S23 is reproduced by the comparator 23. A clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0117]According to this embodiment, it maps each 1 bit of transmitting time stamp information of a 4-bit transmitting time stamp at the transmitting side as mentioned above in every two continuous cells (an odd number cell and an even number cell), When the obstacle in the transmission line of an odd number cell is detected by a receiver, by compensating the information on a receiving time stamp with a loss with reference to the information on the receiving time stamp of an even number cell, Even if single shot cell loss occurs, the loss of a receiving time stamp can be compensated with a data receiver, and the stable reproduction clock can be obtained.

[0118]Although this embodiment explained the case where a 4-bit transmitting time stamp was mapped in eight cells, even if it is not limited to this and changes the bit width and the number of cells of a transmitting time stamp according to a system, the same effect as this embodiment can be acquired.

[0119]What is necessary is to map transmitting time stamp information in two or more cells, and not to just be limited to this, although the case where it mapped each 1 bit of transmitting time stamp information of a transmitting time stamp in every two continuous cells (an odd number cell and an even number cell) was explained.

[0120]For example, as shown in drawing 17, after mapping every 1 bit of transmitting time stamp information of the transmitting time stamp S15 in an odd number cell, it may be made to map the same transmitting time stamp information as the even number cell of the following 8 cell periods. Thereby, also when two or more cells lose, the loss of a receiving time stamp can be compensated by referring to the information on the receiving time stamp of the following 8 cell periods with a data receiver. The same effect can be acquired even if it maps the same transmitting time stamp information in two or more cells regardless of an odd number cell and an even number cell further again.

[0121]Although this specification described each embodiment of the invention separately, naturally it is also possible to combine two or more these composition. Although each embodiment of the invention described ATM communication to the model, the contents of this invention are applicable besides ATM communication.

[0122]
[Effect of the Invention]As mentioned above, the transmitting time stamp generated at the transmitting side which becomes by difference information with the cycle produced by carrying out dividing of the counted value and the source clock which are produced by counting up a network clock according to the source clock playback equipment of this invention is received via a transmission line, The stable reproduction clock can be obtained by amending the receiving time stamp concerned, generating an amendment time stamp, and reproducing a source clock using the

amendment time stamp.

[0123]The calculation difference value which is the difference of two receiving time stamps which are received at intervals of a constant period among two or more above-mentioned receiving time stamps received one by one according to the source clock playback equipment of the next invention, By choosing either of the default difference values set up beforehand, generating an amendment time stamp using the selected difference value concerned, and reproducing a source clock using the amendment time stamp, In any states, it cannot give big disturbance, and it not only can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.

[0124]At the time of a fault occurrence [in / according to the source clock playback equipment of the next invention, it reaches at the time of reset, or / a transmission line]. By choosing the default difference value set up beforehand, generating an amendment time stamp, and reproducing a source clock using the amendment time stamp, Especially, at the time of initial starting, it can reach at the time of cell abolition generating, or cannot give big disturbance at the time of the fault occurrence in a transmission line at the time of reset, and it not only can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.

[0125]When the calculation difference values calculated from two receiving time stamps received at intervals of a constant period among two or more above-mentioned receiving time stamps received one by one are values other than the permission setting range as a time stamp difference value according to the source clock playback equipment of the next invention, By generating an amendment time stamp using the default difference value set up beforehand, and reproducing a source clock using the amendment time stamp, When values other than the permission setting range as a difference value of a time stamp occur especially, and an inaccurate time stamp is received for example, it cannot give big disturbance and it not only can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.

[0126]By according to the source clock playback equipment of the next invention, extending a counter, making an operation clock increase and generating an amendment time stamp using the total difference value adding two or more calculation difference values including the past calculation difference value, Few amendment time stamps with error (change) are generable, and since the error given to a regeneration period can be equalized, the jitter of a reproduction clock is mitigable.

[0127]According to the source clock playback equipment of the next invention, once accumulate a receiving time stamp in a time stamp buffer, read from a buffer according to a reproduction clock, and to a time stamp compensation means by output ******. A receiving time stamp can be prevented from being influenced by the cell delay fluctuation in a transmission line, and disorder of a reproduction clock can be suppressed.

[0128]When according to the data source of the next invention assembling a cell and transmitting using send data and a transmitting time stamp, further again, By mapping the same transmitting time stamp information that constitutes the above-mentioned transmitting time stamp in two or more cells, the loss of a receiving time stamp can be compensated with a receiver, and the reproduction clock stable also at the time of cell abolition generating or a fault occurrence can be obtained.

[0129]According to the data receiver of the next invention, with reference to either of two or more same receiving time stamp information which constitutes a receiving time stamp, the above-mentioned receiving time stamp information is compensated further again, By amending the receiving time stamp concerned, the reproduction clock stable also at the time of cell abolition generating or a fault occurrence can be obtained.

[0130]When according to the data transmission system of the next invention assembling a cell and transmitting using send data and a transmitting time stamp at the transmitting side, further again, The same transmitting time stamp information that constitutes the above-mentioned transmitting time stamp is mapped in two or more cells, The reproduction clock stable also at the time of cell abolition generating or a fault occurrence can be obtained by compensating the above-mentioned receiving time stamp information with reference to either of two or more same receiving time stamp

information that constitutes a receiving time stamp from a receiver, and amending the receiving time stamp concerned.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention]Source clock playback equipment in which this invention reproduces the
source clock frequency of the transmitting side by a receiver, About the data source, a data
receiver, and a data transmission system. For example, the source clock in the data source is
transmitted with a time stamp, and it is related with the source clock playback equipment which
reproduces a source clock from the time stamp with a data receiver, and the data transmission
system using the source clock playback equipment.

[Translation done.]

PRIOR ART

[Description of the Prior Art]In recent years, the demand to the improvement in the speed to a
network and multimedia-izing increases, and introduction of ATM (Asynchronous Transfer Mode;
Asynchronous Transfer Mode) art is advanced. However, on the other hand, there is STM circuit
service of existing, such as voice communication and a teleconference, and it is necessary with the
spread of ATM networks to accommodate these circuit services to an ATM network. In order to
realize said circuit STM circuit service via an ATM network, the art, i.e., source clock reproduction
art, of synchronizing the clock of a circuit by the transmitting side and a receiver is needed.
[0003]As conventional source clock reproduction art, there is a clock reproduction circuit indicated
by JP,8-8918,A, for example. Drawing 18 is a block diagram showing the composition of the
conventional clock reproduction circuit. Operation is explained using drawing 18.
[0004]In the SAR (Segmentation And Reassembly sublayer) header separation part 1, reception of
the cell which is transmitted data transmitted by the ATM transmission system S1 will separate the
SAR header S2. The SAR header S2 separated by the SAR header separation part 1 is constituted
from sequence number protection which protects a sequence number, delta-frequency minute
information, and a sequence number and delta-frequency minute information by the regular format.
[0005]A sequence number is a number series added to a chronological order of a cell in the
transmitting side. The sequence number S3 and delta-frequency minute information S4 are detected
from the SAR header S2 separated by the SAR header separation part 1 by the sequence number
delta-frequency minute information primary detecting element 2. The detected sequence number S3
is supervised by the sequence number Monitoring Department 3, and cell abolition is detected by
the discontinuity of the sequence number S3. And the existence of cell abolition is outputted as the
sequence number monitored result signal S5 from the sequence number Monitoring Department 3.
Management of received delta-frequency minute information S4 is performed by the delta-
frequency part information management forecast processing part 4 with the sequence number
monitored result signal S5.
[0006]When it is usual [which cell abolition or cell delay does not generate] here, With the delta-
frequency part information management signal S6 outputted from the delta-frequency part
information management forecast processing part 4. Received delta-frequency minute information
S4 is recorded instead of the oldest delta-frequency minute information currently recorded on the
memory 5, and the delta-frequency minute information of M cycle eye and the delta-frequency
minute information of a periodic (M-1) eye are recorded on the memory 5.
[0007]When abandonment of the cell which carried out multiplex [of the delta-frequency minute
information of M cycle eye] occurs, the sequence number monitored result signal S5 which
detected generating of cell abolition is outputted from the sequence number Monitoring Department
3 to the delta-frequency part information management forecast processing part 4. Then, the
predicted value of the delta-frequency minute information of M cycle eye is calculated by data
processing using delta-frequency minute information S4 of N cycle eye received correctly before M

cycle eye currently recorded on the memory 5 by the delta−frequency part information management forecast processing part 4, The calculated delta−frequency minute information predicted value S7 is outputted to the clock reproduction part 6. And source clock S9 is reproduced using the delta−frequency minute information predicted value S7 in the clock reproduction part 6.

[0008]As mentioned above, according to the conventional clock reproduction circuit, even when cell abolition occurs in an ATM transmission system, influencing of influence in reproduction of the source clock by this cell abolition can be controlled, it is stabilized and a source clock can be reproduced.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention]As mentioned above, the transmitting time stamp generated at the
transmitting side which becomes by difference information with the cycle produced by carrying out
dividing of the counted value and the source clock which are produced by counting up a network
clock according to the source clock playback equipment of this invention is received via a
transmission line, The stable reproduction clock can be obtained by amending the receiving time
stamp concerned, generating an amendment time stamp, and reproducing a source clock using the
amendment time stamp.
[0123]The calculation difference value which is the difference of two receiving time stamps which
are received at intervals of a constant period among two or more above-mentioned receiving time
stamps received one by one according to the source clock playback equipment of the next
invention, By choosing either of the default difference values set up beforehand, generating an
amendment time stamp using the selected difference value concerned, and reproducing a source
clock using the amendment time stamp, In any states, it cannot give big disturbance, and it not only
can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.
[0124]At the time of a fault occurrence [in / according to the source clock playback equipment of
the next invention, it reaches at the time of reset, or / a transmission line]. By choosing the default
difference value set up beforehand, generating an amendment time stamp, and reproducing a source
clock using the amendment time stamp, Especially, at the time of initial starting, it can reach at the
time of cell abolition generating, or cannot give big disturbance at the time of the fault occurrence in
a transmission line at the time of reset, and it not only can obtain the reproduction clock stable at
the time of normal, but can obtain a reproduction clock.
[0125]When the calculation difference values calculated from two receiving time stamps received at
intervals of a constant period among two or more above-mentioned receiving time stamps received
one by one are values other than the permission setting range as a time stamp difference value
according to the source clock playback equipment of the next invention, By generating an
amendment time stamp using the default difference value set up beforehand, and reproducing a
source clock using the amendment time stamp, When values other than the permission setting range
as a difference value of a time stamp occur especially, and an inaccurate time stamp is received for
example, it cannot give big disturbance and it not only can obtain the reproduction clock stable at
the time of normal, but can obtain a reproduction clock.
[0126]By according to the source clock playback equipment of the next invention, extending a
counter, making an operation clock increase and generating an amendment time stamp using the
total difference value adding two or more calculation difference values including the past calculation
difference value, Few amendment time stamps with error (change) are generable, and since the error
given to a regeneration period can be equalized, the jitter of a reproduction clock is mitigable.
[0127]According to the source clock playback equipment of the next invention, once accumulate a
receiving time stamp in a time stamp buffer, read from a buffer according to a reproduction clock,

and to a time stamp compensation means by output ******. A receiving time stamp can be prevented from being influenced by the cell delay fluctuation in a transmission line, and disorder of a reproduction clock can be suppressed.

[0128]When according to the data source of the next invention assembling a cell and transmitting using send data and a transmitting time stamp, further again, By mapping the same transmitting time stamp information that constitutes the above-mentioned transmitting time stamp in two or more cells, the loss of a receiving time stamp can be compensated with a receiver, and the reproduction clock stable also at the time of cell abolition generating or a fault occurrence can be obtained.

[0129]According to the data receiver of the next invention, with reference to either of two or more same receiving time stamp information which constitutes a receiving time stamp, the above-mentioned receiving time stamp information is compensated further again, By amending the receiving time stamp concerned, the reproduction clock stable also at the time of cell abolition generating or a fault occurrence can be obtained.

[0130]When according to the data transmission system of the next invention assembling a cell and transmitting using send data and a transmitting time stamp at the transmitting side, further again, The same transmitting time stamp information that constitutes the above-mentioned transmitting time stamp is mapped in two or more cells, The reproduction clock stable also at the time of cell abolition generating or a fault occurrence can be obtained by compensating the above-mentioned receiving time stamp information with reference to either of two or more same receiving time stamp information that constitutes a receiving time stamp from a receiver, and amending the receiving time stamp concerned.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, the conventional clock reproduction circuit had
the problem that the reproduction clock of a receiver was confused at the time of initial starting of
a device provided with the clock reproduction circuit. That is, the conventional clock reproduction
circuit reproduces a clock using the delta-frequency minute information memorized at the time of
normal [above-mentioned], when the delta-frequency minute information received when [normal]
cell abolition or cell delay did not occur is memorized and cell abolition, cell delay, etc. occur.
Therefore, since it is in the state before delta-frequency minute information is memorized by the
receiver at the time of initial starting, a reproduction clock is confused.
[0010]The problem that a jitter certainly occurred was among the reproduction clocks reproduced
by a receiver. That is, in an ATM transmission system, since the delta-frequency minute information
used when reproducing a clock is approximated in digital one at the transmitting side, it cannot
coincide a reproduction clock with the clock of the transmitting side thoroughly.
[0011]It was made in order to solve the above problems, and this invention is what kind of state (at
the time of normal.). At the time of initial starting, at the time of a fault occurrence at the time of
cell abolition generating at the time of reset At the time of inaccurate time stamp reception.
Disorder of a reproduction clock can be suppressed also in the time of cell delay, etc., and it aims at
obtaining the source clock playback equipment, the data source, data receiver, and data
transmission system which can reduce the jitter of a reproduction clock.

[Translation done.]

MEANS

[Means for Solving the Problem]Source clock playback equipment of this invention is characterized
by comprising:
It generates at the transmitting side which becomes by difference information with a cycle produced
by carrying out dividing of counted value and a source clock which are produced by counting up a
network clock, A time stamp compensation means which receives a time stamp transmitted via a
transmission line, amends the received time stamp concerned, and outputs an amendment time
stamp.
A counter which counts up the above-mentioned network clock and outputs counted value.
A comparator which reproduces the above-mentioned cycle using an amendment time stamp
outputted from the above-mentioned time stamp compensation means, and counted value outputted
from the above-mentioned counter, and outputs a regeneration period.
A PLL circuit which reproduces the above-mentioned source clock using a regeneration period
outputted from the above-mentioned comparator, and outputs a reproduction clock.

[0013]Source clock playback equipment concerning the next invention, A difference calculation
circuit which calculates difference of two time stamps received at intervals of a constant period
among two or more above-mentioned time stamps received one by one to a time stamp
compensation means which outputs the above-mentioned amendment time stamp, and outputs the
calculation difference value concerned to it, A default output means to output a default difference
value set up beforehand, A selector which chooses default either a calculation difference value
outputted from the above-mentioned difference calculation circuit or a difference value outputted
from the above-mentioned default output means, and is outputted as a difference value, A
difference value outputted to the above-mentioned amendment time stamp outputted last time from
the above-mentioned selector is added, and it has an adding machine which generates a new
amendment time stamp recursively and outputs it.
[0014]Source clock playback equipment concerning the next invention, It has a detection means to
attain to the above-mentioned time stamp compensation means at the time of reset, or to output a
detecting signal to the above-mentioned selector at the time of a fault occurrence in the above-
mentioned transmission line, and the above-mentioned selector is constituted so that the above-
mentioned default difference value may be chosen based on a detecting signal outputted from the
above-mentioned detection means.
[0015]Source clock playback equipment concerning the next invention, It is judged whether a
calculation difference value outputted to the above-mentioned time stamp compensation means
from the above-mentioned difference calculation circuit is a value of a predetermined permission
setting range, When it is values other than the above-mentioned predetermined permission setting
range, it has a difference judging means which outputs an unjust detecting signal to the above-
mentioned selector, and the above-mentioned selector is constituted so that the above-mentioned

default difference value may be chosen based on an unjust detecting signal outputted from the above-mentioned difference judging means.

[0016]Source clock playback equipment concerning the next invention, A difference calculation circuit which calculates difference of two time stamps received at intervals of a constant period among two or more above-mentioned time stamps received one by one to a time stamp compensation means which outputs the above-mentioned amendment time stamp, and outputs the calculation difference value concerned to it, A register which memorizes a calculation difference value outputted from the above-mentioned difference calculation circuit, The 1st adding machine that adds two or more calculation difference values including a calculation difference value memorized by the above-mentioned register, and outputs the total difference value, Add the total difference value outputted to the above-mentioned amendment time stamp outputted last time from the 1st adding machine of the above, has the 2nd adding machine that generates a new amendment time stamp recursively and outputs it, and the above-mentioned counter considers the above-mentioned network clock as an input, It has a clock generating means which generates a clock corresponding to the number of calculation difference values added with the 1st adding machine of the above, and it is constituted so that it may count up with a clock generated by the above-mentioned clock generating means and counted value may be outputted.

[0017]Source clock playback equipment concerning the next invention once accumulates a time stamp received [above-mentioned], and is provided with a time stamp buffer which outputs the time stamp concerned to the above-mentioned time stamp compensation means according to a reproduction clock outputted from the above-mentioned PLL circuit.

[0018]Further again the data source concerning the next invention, A transmitting time stamp creating means which generates a time stamp which becomes by difference information with a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock, When assembling two or more cells and transmitting using two or more transmission data and a time stamp generated by the above-mentioned transmitting time stamp creating means, it has a cell assembly section which maps the same time stamp information that constitutes the above-mentioned time stamp in two or more cells.

[0019]Further again a data receiver concerning the next invention, A cell containing a time stamp which becomes by difference information with a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock, and transmission data is received via a transmission line, A cell decomposition part which decomposes the cell concerned and outputs a time stamp and transmission data, The above-mentioned time stamp information is compensated with reference to either of two or more same time stamp information that constitutes a time stamp outputted from the above-mentioned cell decomposition part, A time stamp compensation means which amends the time stamp concerned and outputs an amendment time stamp, A counter which counts up the above-mentioned network clock and outputs counted value, A comparator which reproduces the above-mentioned cycle using an amendment time stamp outputted from the above-mentioned time stamp compensation means, and counted value outputted from the above-mentioned counter, and outputs a regeneration period, A PLL circuit which reproduces the above-mentioned source clock using a regeneration period outputted from the above-mentioned comparator, and outputs a reproduction clock, Transmission data outputted from the above-mentioned cell decomposition part is once stored, and it has a buffer which outputs the transmission data concerned according to a reproduction clock outputted from the above-mentioned PLL circuit.

[0020]Further again a data transmission system concerning the next invention, A transmitting time stamp creating means which generates a time stamp which becomes by difference information of a cycle produced by carrying out dividing of counted value and a source clock which are produced by counting up a network clock to the data source, When assembling a cell and transmitting using transmission data and a time stamp generated by the above-mentioned transmitting time stamp

creating means, It has a cell assembly section which maps the same time stamp information that constitutes the above-mentioned time stamp in two or more cells, A cell decomposition part which is assembled by the above-mentioned cell assembly section by data receiver, decomposes into it a cell transmitted via a transmission line, and outputs a time stamp and transmission data to it, The above-mentioned time stamp information is compensated with reference to either of two or more same time stamp information that constitutes a time stamp outputted from the above-mentioned cell decomposition part, A time stamp compensation means which amends the time stamp concerned and outputs an amendment time stamp, A comparator which reproduces the above-mentioned cycle using a counter which counts up the above-mentioned network clock and outputs counted value, and an amendment time stamp outputted from the above-mentioned time stamp compensation means and counted value outputted from the above-mentioned counter, and outputs a regeneration period, A PLL circuit which reproduces the above-mentioned source clock using a regeneration period outputted from the above-mentioned comparator, and outputs a reproduction clock, Transmission data outputted from the above-mentioned cell decomposition part is once stored, and it has a buffer which outputs the transmission data concerned according to a reproduction clock outputted from the above-mentioned PLL circuit.

[0021]
[Embodiment of the Invention]Below embodiment 1. describes an embodiment of the invention using a drawing. In an embodiment, a transmitting time stamp and the time stamp received are explained for the time stamp transmitted, and send data and the transmission data received are explained for a receiving time stamp and the transmission data transmitted as received data.

[0022]Drawing 1 is a block diagram showing the composition of the data transmission system concerning the 1 embodiment of this invention. In drawing 1, 10 is the data source which performs data communications in an ATM network, and 20 is a data receiver.

[0023]11 is counted up with the network clock S11, it is a counter which outputs the counted value S13, and four bit counters are used for it here. 12 carries out dividing of the source clock S12, is a counting-down circuit which generates a predetermined periodical pulse, and outputs periodic T S14 as a periodical pulse here.

[0024]13 latches the counted value S13 outputted from the four above-mentioned bit counter 11 every cycle T S14 of the above-mentioned periodical pulse generated with the above-mentioned counting-down circuit 12 (maintenance), He is the latch who outputs the transmitting time stamp S15 which is the difference information of periodic TS14 produced by carrying out dividing of the above-mentioned network clock S11 and the above-mentioned source clock S12. In this embodiment, a transmitting time stamp creating means comprises the four above-mentioned bit counter 11, the counting-down circuit 12, and the latch 13.

[0025]14 is a cell assembly section which assembles the cell S16 and transmits using the send data S10 and the transmitting time stamp S15 outputted by the above-mentioned latch 13. 15 is a transmission line which transmits the cell S16 assembled by the above-mentioned cell assembly section 14.

[0026]21 is a cell decomposition part which decomposes the cell S16 transmitted from the above-mentioned data source 10 via the above-mentioned transmission line 15, and outputs the received data S20 and the receiving time stamp S21. 22 is a time stamp compensation means which calculates the difference of the two receiving time stamps S21 which continue among the receiving time stamps S21 outputted one by one from the above-mentioned cell decomposition part 21, and amends and outputs the amendment time stamp S22 using the difference value.

[0027]While the enable signal S24 outputted from the comparator mask counter 24 which 23 mentions later is asserted, Coincidence detection of the counter value S13 outputted from the four bit counters 11 of the data receiver 20 and the amendment time stamp S22 outputted from the above-mentioned time stamp compensation means 22 is compared and carried out, It is a comparator which reproduces periodic T S14 outputted from the above-mentioned counting-down

circuit 12, and outputs regeneration period Tr S23.

[0028]It is a comparator mask counter which makes operation of the above-mentioned comparator 23 fixed time invalidity, if 24 is counted up with the network clock S11 and a predetermined threshold is exceeded, it will assert the enable signal S24, and if regeneration period Tr S23 is outputted from the above-mentioned comparator 23, it will reset a count.

[0029]25 is a PLL circuit (PhaseLock Loop circuit) which reproduces a clock and outputs the reproduction clock S25 by a phase feedback loop using regeneration period Tr S23 outputted from the above-mentioned comparator 23. 26 is a buffer which outputs the received data S26 according to the reproduction clock S25 which once accumulates the received data S20 outputted from the above-mentioned cell decomposition part 21, and is outputted from above-mentioned PLL circuit 25.

[0030]Next, operation is explained. Although the case where the source clock S12 is 1.544 MHz is explained as an example for simplification, the range of source clock frequency is not limited. Although the basic transmission rates in an ATM network are 155.52Mbps or 622.08Mbps, according to TTC standard JT-I363, when frequency of fn and the source clock S12 is set to fs, there is restriction of 1<fn/fs<=2 about the frequency of the network clock S11.

[0031]For this reason, the frequency of the network clock S11 sets 155.52 MHz to 2.43 MHz which 2 squared −6 here. Although the case where bit width of a time stamp is set to 4 is explained based on TTC standard JT-I363, using the four bit counters 11 as a counter, it cannot be overemphasized that it may be the bit width of the other counter and a time stamp.

[0032]In the data source 10, the counted value S13 unconditionally counted up with the network clock S11 is first outputted from the four bit counters 11. Periodic T S14 produced from the counting-down circuit 12 by carrying out dividing of the source clock S12 on the other hand is outputted. In this embodiment, this periodic T S14 is a data forwarding period for eight cells.

[0033]Then, the counted value S13 which is outputted from the above-mentioned counting-down circuit 12 by the latch 13 and which is outputted from the above-mentioned bit counter 11 every cycle T S14 is latched, and it is outputted to the cell assembly section 14 as the transmitting time stamp S15.

[0034]In this embodiment, the value of a transmitting time stamp is the remainder which added the value of the last transmitting time stamp to the periodicity of the cycle T by network clock conversion, and was divided by 16. As mentioned above, periodic T S14 is equivalent to the sending-out period for eight cells of the cell S16, and is a part for 3008 clocks of source clock frequency, i.e., 1.948 ms. The value will be set to 4733 or 4334 if network clock conversion of this is carried out. The value of the last transmitting time stamp is added to this value, and the remainder divided by 16 serves as a value of this transmitting time stamp.

[0035]If the transmitting time stamp S15 is outputted to the cell assembly section 14 from the above-mentioned latch 13, in the cell assembly section 14, the cell S16 will be assembled using the transmission data S10 and the above-mentioned transmitting time stamp S15, and the cell S16 will be sent out to the data receiver 20 via the transmission line 15.

[0036]Drawing 2 is a key map showing the composition of the cell of the 53-byte length by the AAL (ATM adaptation layer) type 1. 5 bytes of ATM header in which D1 stores the header information of ATM transmission in drawing 2, 1 byte of SAR-PDU header in which D2 stores the header information of transmitted data (Segmentation And Reassembly-Protocol Data Unit header), The SAR-PDU pay load in which D3 stores send data, the CSI bit in which D4 stores a time stamp (Convergence Sublayer Indication bit), SC field (Sequence field) where D5 stores a sequence number, the CRC field (Cycric Redundancy Check field) which uses D6 for a Cyclic Redundancy Check, and D7 are even parity used for a parity check.

[0037]The send data S10 is mapped by the SAR-PDU pay load D3, the transmitting time stamp S15 is mapped by CSI bit D4, respectively, and the cell S16 is assembled by the cell assembly section 14.

[0038]Drawing 3 is a key map showing the example which seems to map a transmitting time stamp in the cell S16 in the cell assembly section 14. In the case of drawing 3, the 4-bit transmitting time stamp S15 is divided into every 1 bit of transmitting time stamp information, and the SC field D5 is mapped by CSI bit D4 of the cell whose number is odd among the eight cells S16.

[0039]Next, the data receiver 20 is explained. First, the cell S16 transmitted from the data source 10 is decomposed by the cell decomposition part 21, the received data S20 are outputted to the buffer 26, and the receiving time stamp S21 is outputted to the time stamp compensation means 22.

[0040]In [if the above-mentioned receiving time stamp S21 is outputted to the time stamp compensation means 22] the time stamp compensation means 22, The difference of the last above-mentioned receiving time stamp S21 and this receiving time stamp S21 is calculated among the receiving time stamps S21 inputted one by one, and the amendment time stamp S22 amended using the difference value is outputted to the comparator 34. Detailed operation of the time stamp compensation means 22 is mentioned later.

[0041]On the other hand, from the four bit counters 11, the counted value S13 unconditionally counted up with the network clock S11 is outputted to the comparator 23. If it counts up with the network clock S11 and a threshold is exceeded until it exceeds a threshold at the comparator mask counter 24 simultaneously with this, the enable signal S24 will be asserted.

[0042]While the above-mentioned enable signal S24 is asserted, by the comparator 23. Coincidence detection of the counted value S13 outputted from the four above-mentioned bit counter 11 and the amendment time stamp S22 outputted from the above-mentioned time stamp compensation means 22 is performed, periodic T S14 outputted from the above-mentioned counting-down circuit 12 is reproduced from the result, and regeneration period TrS23 is outputted.

[0043]Here, a value a little smaller than the minimum which periodic T S14 can take is used for the threshold of the above-mentioned comparator mask counter 24. For example, when the transfer characteristic of the source clock S12 with a frequency of 1.544 MHz sets to **100 ppm, periodic T S14 is a part for 4733 to 4735 clock in network clock S11 conversion. Therefore, what is necessary is just to choose about 4730 as the above-mentioned threshold. By doing this way, the comparator 23 can obtain regeneration period Tr S23.

[0044]And if regeneration period TrS23 is outputted from the above-mentioned comparator 23, the comparator mask counter 24 will be reset. If regeneration period Tr S23 outputted from the above-mentioned comparator 23 is inputted into PLL circuit 25, a clock will be reproduced by the phase feedback loop in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 will be outputted. Then, according to the reproduction clock S25, the received data S26 are outputted from the above-mentioned buffer 26. Thus, periodic T S14 of the data source 10 can be reproduced as regeneration period Tr S23 with the data receiver 20, and received data can be read.

[0045]Next, the above-mentioned time stamp compensation means 22 which is a main part of this embodiment is explained in detail. Drawing 4 is a block diagram showing the composition of the above-mentioned time stamp compensation means 22. In drawing 4, 31 is the default difference value S30 set up beforehand a default output means to output, and here, The value "+14" generated most frequently as a difference value of two receiving time stamps which continue among the receiving time stamps S21 outputted one by one from the cell decomposition part 21 is outputted as a default difference value. 32 is a difference calculation circuit which calculates the difference of the two receiving time stamps S21 which continue among the receiving time stamps S21 outputted one by one from the cell decomposition part 21, and outputs the calculation difference value S31.

[0046]33a is a detection means to output a detecting signal, and when the reset signal S32 from the system monitoring part which is not illustrated is detected here and the reset signal S32 is detected, it is a reset signal detection means which outputs the reset detecting signal S33. For example, the above-mentioned system monitoring part 33a outputs the above-mentioned reset

signal S32 at the time of the reset at the time of reset of the device by a user, etc. at the time of the restoration from a line disruption or device failure generating at the time of initial starting of a system.

[0047]34 chooses default either the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 or the difference value outputted from the above-mentioned default output means 31 S30, Based on the reset detecting signal S33 which is a selector outputted as the difference value S34, and is outputted from the above-mentioned reset signal detection means 33a, At the time of reset, the default difference value S30 outputted from the above-mentioned default output means 31 is chosen, and when it is not at the reset time, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen. 35 is an adding machine which adds the difference value S34 outputted to the amendment time stamp S22 outputted last time from the above-mentioned selector 34, generates the new amendment time stamp S22 recursively, and outputs it.

[0048]Operation of the time stamp compensation means 22 is explained. Drawing 5 is a key map showing the concept of operation at the time of normal of the time stamp compensation means 22 by the composition of drawing 4. The receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 is inputted into the difference calculation circuit 32 of the time stamp compensation means 22.

[0049]Then, the default difference value S30 is outputted to the selector 34 from the default output means 31. On the other hand, from the difference calculation circuit 12, the difference of the two receiving time stamps S21 which continue among the receiving time stamps S21 outputted one by one from the above-mentioned cell decomposition part 21 is calculated, and the calculation difference value S31 is outputted to the selector 34.

[0050]For example, when the receiving time stamp S21 "14" is inputted into the difference calculation circuit 32 and the receiving time stamp S21 "12" is inputted last time this time, the calculation difference value S31 is set to "12-14=+14."

[0051]Since the reset signal detection means 33a to the reset detecting signal S33 is not outputted at the time (when it is not at the reset time) of normal, in the selector 34, the calculation difference value S31 outputted from the difference calculation circuit 32 is chosen, and the difference value S34 is outputted to the adding machine 35.

[0052]Then, with the adding machine 35, the difference value S34 outputted from the above-mentioned selector 34 is added to the amendment time stamp S22 outputted last time, and is outputted as this amendment time stamp S22. For example, the calculation difference value S31 outputted from the above-mentioned selector 34 is "+14", and when the amendment time stamp S22 outputted last time is "8", this amendment time stamp S22 is set to "8+(+14) =6."

[0053]Thus, at the time of normal, an amendment time stamp is generated using the calculation difference value S31 calculated from the receiving time stamp S21, and it is outputted to the comparator 23.

[0054]Next, the operation at the time of reset is explained. Drawing 6 is a key map showing the concept of operation at the time of reset of the time stamp compensation means 22 by the composition of drawing 4. In drawing 6, S21a is the receiving time stamp received at the time of reset.

[0055]At the time of reset, while the received receiving time stamp S21a is inputted, the reset signal S32 is detected and the reset detecting signal S33 is outputted to the selector 34 by the reset signal detection means 33a.

[0056]On the other hand, if the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 is inputted into the difference calculation circuit 32 of the time stamp compensation means 22 like the time of normal at the time of reset, The default difference value S30 "+14" is outputted to the selector 34 from the default output means 31, and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 12.

[0057]Then, in the selector 34, the default difference value S30 "+14" outputted from the above-mentioned default output means 31 based on the reset detecting signal S33 outputted from the reset signal detection means 33a is chosen, and this is outputted as the difference value S34.

[0058]And with the adding machine 35, the difference value S34 outputted from the above-mentioned selector 34 is added to the amendment time stamp S22 outputted last time, and is outputted to the comparator 23 as this amendment time stamp S22. Thus, since the default difference value S30 outputted by the selector 34 from the default output means 31 is chosen at the time of reset, the receiving time stamp S21a at the time of reset is not reflected in the amendment time stamp S22.

[0059]The receiving time stamp S21a received at the time of reset has an unstable state of a system, and the timing of reception is changed. It is in the state before receiving the receiving time stamp S21 at the time of initial starting of a system. Therefore, by not reflecting the receiving time stamp S21a at the time of reset in the amendment time stamp S22, since the calculation difference value S31 is correctly incalculable, The time stamp compensation means 22 can generate the amendment time stamp S22 at the time of reset, and the data receiver 20 can reproduce stable regeneration period Tr S23.

[0060]Then, if time passes and a system becomes normal, a reset signal will no longer be detected by the reset signal detection means 33a. Then, the reset detecting signal S33 is no longer outputted from the reset signal detection means 33a, and the calculation difference value S31 outputted from the difference calculation circuit 32 comes to be chosen by the selector 34 like the operation at the above-mentioned time of normal.

[0061]According to this embodiment, the stable reproduction clock can be obtained as mentioned above by amending a receiving time stamp using the calculation difference value calculated from two continuous receiving time stamps, and generating an amendment time stamp with a data receiver.

[0062]A data receiver generates an amendment time stamp using the calculation difference value calculated from two receiving time stamps which continue at the time of normal, By generating an amendment time stamp using the default difference value beforehand set up at the time of reset, and reproducing the source clock of the transmitting side using the amendment time stamp, the time of the reset which it not only can obtain the reproduction clock stable at the time of normal, but includes the time of initial starting of a system — being also alike — big disturbance cannot be given and a reproduction clock can be obtained.

[0063]Although this embodiment explained the case where a calculation difference value was calculated from two continuous receiving time stamps, it is not limited to this. The calculation difference value is just a difference value of the receiving time stamp of a constant period interval, for example, may be a difference value of the receiving time stamp in every other one. In this case, although time until a reproduction clock is stabilized increases somewhat, the jitter of a reproduction clock is mitigable.

[0064]Although the embodiment of the embodiment 2. above-mentioned can form the reset signal detection means 33a in the time stamp compensation means 22 and the reproduction clock stable also at the time of reset can be obtained, Next, the embodiment which can obtain the reproduction clock stable when the obstacle in a transmission line occurred is shown.

[0065]Drawing 7 is a block diagram showing the composition of the time stamp compensation means 22 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. 13b is a detection means to output a detecting signal to the selector 34, and when the sequence number S35 of the cell stored in the SC field D5 shown in drawing 2 here is supervised, an obstacle is detected and an obstacle is detected, it is a fault detection means which outputs the failure detection signal S33 to the selector 34. Here, the sequence number S35 is inputted from the cell decomposition part 21 shown in drawing 1. An obstacle is an obstacle in a transmission line detectable from the sequence number S35, and are obstacles that the cell erroneous insertion which the cell loss (cell abolition) to

which a cell does not reach a receiver, and an unnecessary cell reach, and an attainment order of a cell are confused, such as a sequence error.

[0066]Based on the failure detection signal S33 outputted from the above-mentioned fault detection means 33b, the selector 34, The default difference value S30 outputted from the above-mentioned default output means 31 is chosen, at the time of a fault occurrence, when it is not at the reset time, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and it outputs the difference value S34.

[0067]Operation is explained. Drawing 8 is a key map showing the concept of operation at the time of the fault occurrence of the time stamp compensation means 22 by the composition of drawing 7. In drawing 8, S21b is the time stamp lost at the time of a fault occurrence, and shows that a time stamp did not reach to a data receiver.

[0068]At the time of normal, an obstacle is not detected and the failure detection signal S33 is not outputted to the selector 34 by the obstacle inspection means 33b (when an obstacle does not occur). Therefore, after the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 was inputted into the difference calculation circuit 32 of the time stamp compensation means 22, If the default difference value S30 is outputted to the selector 34 from the default output means 31 and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 32, In the selector 34, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and this is outputted to the adding machine 35 as the difference value S34.

[0069]That is, while the receiving time stamp S21 is normally transmitted with "3, 1, 14", the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen by the selector 34, and "+13, +14" are outputted in order to the adding machine 35 as the difference value S34.

[0070]On the other hand, at the time of a fault occurrence, an obstacle is detected from the sequence number S35, and the failure detection signal S33 is outputted to the selector 34 by the obstacle inspection means 33b. Then, after the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 was inputted into the difference calculation circuit 32 of the time stamp compensation means 22, If the default difference value S30 is outputted to the selector 34 from the default output means 31 and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 32, The default difference value S30 outputted from the above-mentioned default output means 31 is chosen by the selector 34, and this is outputted to the adding machine 35 as the difference value S34.

[0071]That is, when a receiving time stamp does not reach like the lost time stamp S21b, the default difference value S30 "+14" outputted from the above-mentioned default output means 31 is chosen by the selector 34, and "+14" is outputted to the adding machine 35 as the difference value S34.

[0072]If the difference value S34 is outputted to the adding machine 35 from the above-mentioned selector 34, like the above-mentioned embodiment, the amendment time stamp S22 will be generated by the adding machine 35, and it will be outputted to the comparator 23. Regeneration period Tr S23 is reproduced using the above-mentioned amendment time stamp S22 by the comparator 23, a clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0073]According to this embodiment, a data receiver generates an amendment time stamp using the calculation difference value calculated from two receiving time stamps which continue at the time of normal as mentioned above, By generating an amendment time stamp using the default difference value beforehand set up at the time of a fault occurrence, and reproducing the source clock of the transmitting side using the amendment time stamp, At the time of a fault occurrence, when an obstacle occurs in a transmission line and a time stamp does not arrive for example, it cannot give big disturbance and it not only can obtain the reproduction clock stable at the time of normal, but

can obtain a reproduction clock.

[0074]Although this embodiment explained the case where a calculation difference value was calculated from two continuous receiving time stamps, the calculation difference value should just be a difference value of the receiving time stamp of a constant period interval, and it cannot be overemphasized that it is not what is limited to this.

[0075]Although the reproduction clock stable at the time of reset and a fault occurrence can be obtained in the embodiment of the embodiment 3. above-mentioned next, the embodiment which can obtain the reproduction clock stable when an inaccurate time stamp was received is shown.

[0076]Drawing 9 is a block diagram showing the composition of the time stamp compensation means 22 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. 33c supervises the calculation difference value S32 outputted from the difference calculation circuit 12, It is a difference judging means which judges whether the calculation difference value S32 is a value of the permission setting range as a difference value of a time stamp, judges with having received the time stamp inaccurate when it is values other than a permission setting range, and outputs the unjust detecting signal S33 to the selector 34. For example, the permission setting range as a time stamp difference value is set as +13–+15.

[0077]Based on the unjust detecting signal S33 outputted from the above-mentioned difference judging means 33c, the selector 34, When values other than the permission setting range as a time stamp difference value occur, the default difference value S30 outputted from the above-mentioned default output means 31 is chosen, when other, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and the difference value S34 is outputted.

[0078]Operation is explained. In the time stamp compensation means 22 by the composition of drawing 9, drawing 10 is a key map showing a concept of operation when values other than the permission setting range as a time stamp difference value occur.

[0079]If the receiving time stamp S21 outputted from the above-mentioned cell decomposition part 21 is inputted into the difference calculation circuit 32 of the time stamp compensation means 22 like the above-mentioned embodiment, The default difference value S30 is outputted to the selector 34 from the default output means 31, and the calculation difference value S31 is outputted to the selector 34 from the difference calculation circuit 32.

[0080]It can come, simultaneously the calculation difference value S31 from the above-mentioned difference calculation circuit 32 is outputted to the difference judging means 33c. Then, it is judged whether the above-mentioned calculation difference value S31 is a value of the permission setting range as a difference value of a time stamp in the difference judging means 33c.

[0081]As a result, when the above-mentioned calculation difference value S31 is a value in a permission setting range, it is not judged with having received the inaccurate time stamp, and the unjust detecting signal S33 is not outputted from the difference judging means 33c. In this case, in the selector 34, the calculation difference value S31 outputted from the above-mentioned difference calculation circuit 32 is chosen, and this is outputted to the adding machine 35 as the difference value S34. That is, when the difference value of the two continuous receiving time stamps S21 is +13–+15, the above-mentioned calculation difference value S31 is chosen by the selector 34.

[0082]On the other hand, when the above-mentioned calculation difference values S31 are values other than a permission setting range, it judges with having received the inaccurate time stamp, and the unjust detecting signal S33 is outputted to the selector 34 from the above-mentioned difference judging means 33c. Then, in the selector 34, the default difference value S30 outputted from the above-mentioned default output means 31 based on the above-mentioned unjust detecting signal S33 is chosen, and it is outputted to the adding machine 35 as the difference value S34.

[0083]That is, for example, in drawing 10, the last receiving time stamp S21 is "14", and when this

receiving time stamp S21 is "9", the calculation difference value S31 is set to "14-9=+11." However, since "+11" is outside the range of a permission setting range (+13-+15), the unjust detecting signal S33 is outputted to the selector 34 from the above-mentioned difference judging means 33c, and the above-mentioned default difference value S30 "+14" is chosen based on the above-mentioned unjust detecting signal S33 in the selector 34.

[0084]If the difference value S34 is outputted to the adding machine 35 from the above-mentioned selector 34, like the above-mentioned embodiment, the amendment time stamp S22 will be generated by the adding machine 35, and it will be outputted to the comparator 23. Regeneration period Tr S23 is reproduced using the above-mentioned amendment time stamp S22 by the comparator 23, a clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0085]As mentioned above, when the calculation difference values calculated from two continuous receiving time stamps are values other than the permission setting range as a time stamp difference value according to this embodiment, By generating an amendment time stamp using the default difference value set up beforehand, and reproducing the source clock of the transmitting side using the amendment time stamp, When values other than the permission setting range as a difference value of a time stamp occur, and inaccurate time stamp is received for example, it cannot give big disturbance and it not only can obtain the reproduction clock stable at the time of normal, but can obtain a reproduction clock.

[0086]Although this embodiment explained the case where a calculation difference value was calculated from two continuous receiving time stamps, the calculation difference value should just be a difference value of the receiving time stamp of a constant period interval, and it cannot be overemphasized that it is not what is limited to this.

[0087]Although an amendment time stamp is generated from one difference value next, the embodiment of the embodiment 4. above-mentioned extends the number of bits of the counter of a data receiver, makes an operation clock increase, and shows the embodiment which generates an amendment time stamp from two or more difference values.

[0088]Drawing 11 is a block diagram showing the composition of the time stamp compensation means 22 concerning this embodiment. In drawing 11, identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted.

[0089]36 is a register outputted as the calculation difference value S36 of 1 time ago, when the calculation difference value S31 outputted from the difference calculation circuit 32 is memorized and the following calculation difference value S31 is further outputted from the above-mentioned difference calculation circuit 32.

[0090]37 is the 1st adding machine that adds the calculation difference value S36 before [one] being outputted from the calculation difference value S31 and the above-mentioned register which are outputted from the above-mentioned difference calculation circuit 32, and outputs the total difference value S37. 38 is an adding machine which adds the total difference value S37 outputted to the amendment time stamp S22 outputted last time from the 1st adding machine 37 of the above, generates the new amendment time stamp S22 recursively, and outputs it.

[0091]Drawing 12 is a block diagram showing the composition of the data receiver 20 concerning this embodiment. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. 27 is a clock generating means which generates the clock corresponding to the number of the calculation difference values added with the 1st adding machine of the above by considering the network clock S11 as an input. Here, since two calculation difference values are added with the 1st adding machine of the above, the clock which is twice the network clock is generated.

[0092]28 is the counted value S22 counted up with the clock generated by the above-mentioned clock generating means 27 an extended counter to output, and here, Since an operation clock (network clock) doubles by the above-mentioned clock generating means 27, five bit counters which

carried out 1 bit extension of the four bit counters are used. In this embodiment, a counter comprises the above-mentioned clock generating means 27 and five above-mentioned bit counter. Like the above-mentioned embodiment, although the time stamp compensation means 22 generates the amendment time stamp S22, it generates the amendment time stamp corresponding to 5 bits here.

[0093]Operation is explained. Drawing 13 is a key map showing the concept of operation of the time stamp compensation means 22 in this case. Identical codes are given to a portion the same as that of the above-mentioned embodiment, or considerable, and explanation is omitted. S31 is the calculation difference value outputted from the difference calculation circuit 32, and is outputted in order of a, b, and c. S36 is the last calculation difference value outputted from the register 36 according to the timing to which the above-mentioned calculation difference value S31 is outputted, and d, e, and f are the same as the above-mentioned a, b, and c respectively. S37 is the total difference value outputted from the 1st adding machine 37 of the above.

[0094]First, like the above-mentioned embodiment, if the receiving time stamp S21 is inputted into the difference calculation circuit 32, the calculation difference value S31 will be outputted. In an initial state, the calculation difference value S31a "+14" is memorized by the register 36 as the last calculation difference value S36d "+14."

[0095]And if the following receiving time stamp S21 is inputted into the difference calculation circuit 32, the calculation difference value S31b "+14" will be outputted from the difference calculation circuit 32, and it will be inputted into the 1st adding machine 37. It can come, simultaneously with the last calculation difference value S36d "+14" is outputted from the above-mentioned register 36, and it is inputted into the 1st adding machine 37.

[0096]Then, the above-mentioned calculation difference value S31b "+14" and the last above-mentioned calculation difference value S36d "+14" are added with the 1st adding machine 37, and the total difference value S37g "+28" is inputted into the 2nd adding machine 38. In the 2nd adding machine 38, the total difference value S37g "+28" is added to the amendment time stamp "11" outputted last time, and the new amendment time stamp S22 "7" is outputted.

[0097]By thus, the thing for which the amendment time stamp S22 corresponding to an extension bit is generated from the total difference value S37 adding this calculation difference value S31 and the last calculation difference value S36. Equalizing the error (change) of an amendment time stamp and equalizing the error given to regeneration period Tr S23 can carry out, and the jitter of the reproduction clock S25 can be reduced.

[0098]That is, since a time stamp is approximated in digital one at the transmitting side, disorder arises in a calculation difference value in a receiver. For example, in the calculation difference value S31, only the calculation difference value S31c is set to "+13." For this reason, when not extending the amendment time stamp of a receiver, a gap arises in an amendment time stamp in this portion, it is confused to regeneration period Tr S23 generated using this amendment time stamp, and a jitter arises in the reproduction clock S25.

[0099]On the other hand, in the case where the amendment time stamp of a receiver is extended, "+27" is repeated twice with the total difference value S37. That is, if "+27" is converted into the usual network clock, it is "+13.5" and the error given to regeneration period Tr S23 can be equalized. Therefore, clock reproduction can be carried out using regeneration period Tr S23 equalized, and the jitter of the reproduction clock S25 can be reduced.

[0100]According to this embodiment, 1 bit extension of the four bit counters of a data receiver is carried out as mentioned above, By making an operation clock increase twice and generating the amendment time stamp corresponding to an extension bit from the total difference value adding this calculation difference value and the last calculation difference value, Few amendment time stamps with error (change) are generable, and since the error given to regeneration period Tr S23 can be equalized, the jitter of a reproduction clock is mitigable.

[0101]Although carried out 1 bit extension of the four bit counters, the operation clock was made to

increase twice and the case where an amendment time stamp was generated from the total difference value of two difference values was explained by this embodiment, it is not limited to this. k (k is natural number) bit extension carries out N (N is natural number) bit counter, an operation clock is made to increase by m times (m is the k–th power of 2), and it may be made to generate an amendment time stamp from the total difference value of the difference value of 2^k individual.

[0102]In this case, a clock generating means is constituted so that the clock corresponding to the number k of extension bits may be generated, and an extended counter uses a N+k bit counter. A time stamp compensation means is made composition as shown in drawing 14, for example. Drawing 14 is a block diagram showing the composition of the time stamp compensation means in the case of using a N+k bit counter, gives identical codes to a portion the same as that of drawing 11, or considerable, and omits explanation.

[0103]36 is a register group which memorizes the calculation difference value outputted from the difference calculation circuit 32, and comprises a register of 2^{k-1} individual mentioned later. 361 is the 1st register outputted as the calculation difference value S361 of 1 time ago, when the calculation difference value S31 outputted from the above–mentioned difference calculation circuit 32 is memorized and the following calculation difference value S31 is further outputted from the above–mentioned difference calculation circuit 32. 362 is the 2nd register outputted as the calculation difference value S362 of 2 times ago, when the calculation difference value S361 before [one] being outputted from the 1st register of the above is memorized and the following calculation difference value S31 is further outputted from the above–mentioned difference calculation circuit 32. Similarly 363 memorizes the calculation difference value in front of 2^{k-2} time outputted from the 2nd $^{k-2}$ register, When the following calculation difference value S31 is furthermore outputted from the above–mentioned difference calculation circuit 32, it is the 2nd $^{k-1}$ register outputted as the calculation difference value S363 in front of 2^{k-1} time.

[0104]Thus, k bit extension the counter of a data receiver by carrying out, making an operation clock increase by m times (m is the k–th power of 2), and generating the amendment time stamp corresponding to a N+k bit from the total difference value adding the calculation difference value of k pieces, Computational complexity and the number of registers increase so that several k of the calculation difference value to add is large, but the jitter of a reproduction clock is more mitigable.

[0105]Although the case where a calculation difference value was calculated from two continuous receiving time stamps was explained, the calculation difference value should just be a difference value of the receiving time stamp of a constant period interval, and it cannot be overemphasized that it is not what is limited to this.

[0106]The embodiment of the embodiment 5. above–mentioned shows the embodiment which generates an amendment time stamp according to cell delay fluctuation, although an amendment time stamp is generated according to the timing which a cell reaches to a data receiver next.

[0107]Drawing 15 is a block diagram showing the composition of the data receiver 20 concerning this embodiment. Identical codes are given to a portion the same as that of the above–mentioned embodiment, or considerable, and explanation is omitted. The buffer 26 comprises a data buffer which accumulates the received data S20 disassembled and outputted by the cell decomposition part 21, and a time stamp buffer which accumulates the receiving time stamp S21, The above–mentioned received data S20 and the receiving time stamp S21 are once accumulated, and the received data S26 and the receiving time stamp S21 are outputted according to the reproduction clock S25 outputted from PLL circuit 25.

[0108]Operation is explained. The cell transmitted from the data source 10 is decomposed into the received data S20 and the receiving time stamp S21 by the cell decomposition part 21, and the received data S20 and the receiving time stamp S21 which were disassembled [above–mentioned] are accumulated in the buffer 26. At this time, 1 or two or more receiving time stamps S21 are accumulated in the buffer 26 according to the situation of cell delay fluctuation of a transmission

line.

[0109]The receiving time stamp S21 accumulated in the above-mentioned buffer 26 is read according to the reproduction clock S25 outputted from PLL circuit 25, and is outputted to the time stamp compensation means 22.

[0110]Henceforth, like the above-mentioned embodiment, the amendment time stamp S22 is outputted to the comparator 23 from the time stamp compensation means 22, and regeneration period Tr S23 is reproduced by the comparator 23. And a clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0111]By once accumulating a receiving time stamp in a buffer, and reading from a buffer according to a reproduction clock according to this embodiment, as mentioned above, A receiving time stamp can be prevented from being influenced by the cell delay fluctuation in a transmission line, and disorder of a reproduction clock can be suppressed.

[0112]When a transmitting time stamp is mapped in a cell by a cell assembly section, a sequence number maps a transmitting time stamp in odd cells (an odd number cell is called hereafter.), but the embodiment of the embodiment 6. above-mentioned. Next, a sequence number maps a transmitting time stamp also in even cells (an even number cell is called hereafter.), and the embodiment with which the loss of a receiving time stamp is compensated is shown.

[0113]Drawing 16 is a key map showing signs that the cell assembly section 14 maps a transmitting time stamp in a cell in this embodiment. Identical codes are given to an above-mentioned embodiment and identical parts, and explanation is omitted. When the cell assembly section 14 assembles a cell and transmits using send data and the transmitting time stamp outputted by the latch 13, it maps the same transmitting time stamp information that constitutes the above-mentioned transmitting time stamp in two or more cells.

[0114]Operation is explained. In the above-mentioned cell assembly section 14, when the 4-bit transmitting time stamp S15 is mapped in eight cells, it maps each 1 bit of transmitting time stamp information of the 4 above-mentioned bits transmitting time stamp S15 in every two continuous cells (an odd number cell and an even number cell). That is, in drawing 16, after mapping 1 bit of transmitting time stamp information of the transmitting time stamp S15 in the odd number cell C1, 1 bit of the same transmitting time stamp information also as the continuing even number cell C2 is mapped. Similarly, every 1 bit of the respectively same transmitting time stamp information as the odd number cell C3, the even number cell C4 and the odd number cell C5, the even number cell C6 and the odd number cell C7, and the even number cell C8 is mapped.

[0115]When the obstacle 33b in a transmission line detectable from a sequence number, for example, the above-mentioned fault detection means, detects the cell loss of an odd number cell, with reference to the information on the receiving time stamp S21 of an even number cell, the loss of the information on a receiving time stamp is compensated with the data receiver 20.

[0116]And the amendment time stamp created using the information on the receiving time stamp which the account of the upper compensated from the time stamp compensation means 22 is outputted to the comparator 23, and regeneration period Tr S23 is reproduced by the comparator 23. A clock is reproduced in PLL circuit 25 using the above-mentioned regeneration period Tr S23, and the reproduction clock S25 is outputted.

[0117]According to this embodiment, it maps each 1 bit of transmitting time stamp information of a 4-bit transmitting time stamp at the transmitting side as mentioned above in every two continuous cells (an odd number cell and an even number cell), When the obstacle in the transmission line of an odd number cell is detected by a receiver, by compensating the information on a receiving time stamp with a loss with reference to the information on the receiving time stamp of an even number cell, Even if single shot cell loss occurs, the loss of a receiving time stamp can be compensated with a data receiver, and the stable reproduction clock can be obtained.

[0118]Although this embodiment explained the case where a 4-bit transmitting time stamp was

mapped in eight cells, even if it is not limited to this and changes the bit width and the number of cells of a transmitting time stamp according to a system, the same effect as this embodiment can be acquired.

[0119]What is necessary is to map transmitting time stamp information in two or more cells, and not to just be limited to this, although the case where it mapped each 1 bit of transmitting time stamp information of a transmitting time stamp in every two continuous cells (an odd number cell and an even number cell) was explained.

[0120]For example, as shown in drawing 17, after mapping every 1 bit of transmitting time stamp information of the transmitting time stamp S15 in an odd number cell, it may be made to map the same transmitting time stamp information as the even number cell of the following 8 cell periods. Thereby, also when two or more cells lose, the loss of a receiving time stamp can be compensated by referring to the information on the receiving time stamp of the following 8 cell periods with a data receiver. The same effect can be acquired even if it maps the same transmitting time stamp information in two or more cells regardless of an odd number cell and an even number cell further again.

[0121]Although this specification described each embodiment of the invention separately, naturally it is also possible to combine two or more these composition. Although each embodiment of the invention described ATM communication to the model, the contents of this invention are applicable besides ATM communication.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the data transmission system concerning the embodiment of the invention 1.
[Drawing 2]It is a key map showing the composition of a cell.
[Drawing 3]It is a key map showing signs that a transmitting time stamp is mapped in a cell in the embodiment of the invention 1.
[Drawing 4]It is a block diagram showing the composition of the time stamp compensation means concerning the embodiment of the invention 1.
[Drawing 5]It is a key map showing the concept of operation at the time of normal of a time stamp compensation means.
[Drawing 6]It is a key map showing the concept of operation at the time of reset of a time stamp compensation means.
[Drawing 7]It is a block diagram showing the composition of the time stamp compensation means concerning the embodiment of the invention 2.
[Drawing 8]It is a key map showing the concept of operation at the time of the fault occurrence of a time stamp compensation means.
[Drawing 9]It is a block diagram showing the composition of the time stamp compensation means concerning the embodiment of the invention 3.
[Drawing 10]It is a key map showing a concept of operation when calculation difference values other than the permission setting range of a time stamp compensation means occur.
[Drawing 11]It is a block diagram showing the composition of the time stamp compensation means concerning the embodiment of the invention 4.
[Drawing 12]It is a block diagram showing the composition of the data receiver concerning the embodiment of the invention 4.
[Drawing 13]It is a key map showing the concept of operation of the time stamp compensation means concerning the embodiment of the invention 4.
[Drawing 14]It is a block diagram showing the composition of the time stamp compensation means in the case of using a N+k bit counter.
[Drawing 15]It is a block diagram showing the composition of the data receiver concerning the embodiment of the invention 5.
[Drawing 16]It is a key map showing signs that it maps in the cell which continues a transmitting time stamp in the embodiment of the invention 6.
[Drawing 17]It is a key map showing signs that a transmitting time stamp is mapped in the cell of eight cycles in the embodiment of the invention 6.
[Drawing 18]It is a block diagram showing the composition of the conventional clock reproduction circuit.
[Description of Notations]

1 SAR header separation part 2 sequence-number delta-frequency minute information primary detecting element
3 Sequence number Monitoring Department Four Delta-frequency part information management forecast processing part
5 Memory Six clock reproduction parts
10 Data source 11 Four bit counters
12 Counting-down circuit 13 Latch
14 Cell assembly section 15 Transmission line
20 Data receiver 21 Cell decomposition part
22 Time stamp compensation means 23 Comparator
24 Comparator mask counter 25 PLL circuits
26 Buffer 27 clock generating means
28 Five bit counters 31 default output means
32 Difference calculation circuit 33a Reset signal detection means
33b Fault detection means 33c Difference judging means
34 Selector 35 Adding machine
36 Register 37 The 1st adding machine
38 The 2nd adding machine C0-C15 Cell

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.
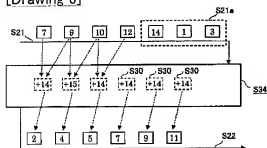
DRAWINGS

[Drawing 1]

[Drawing 2]

6 Byte	ATM Header
1 Byte	
47 Byte	SAR-PDU payload

SAR-PDU Header

CSI bit | SC field | CRC field | Even parity

[Drawing 3]

タイムスタンプ

4bit MSB列

S15

S16

C7 C6 C5 C4 C3 C2 C1 C0

[Drawing 4]

デフォルト出力手段 31

差分計算回路 32

リセット信号検出手段 33a

セレクタ 34

加算器 35

差分値

S21 S30 S34 S22

S32 S31 S33

22

[Drawing 5]

S21 | 7 | 9 | 10 | 12 | 14 | 1 | 3

+14 +15 +14 +14 +15 +14 S31

S34

1 | 3 | 4 | 6 | 8 | 11 | S22

[Drawing 6]

S21a

S21 | 7 | 9 | 10 | 12 | 14 | 1 | 3

+14 +15 +14 S30 S30 S30

S34

2 | 4 | 5 | 7 | 9 | 11 | S22
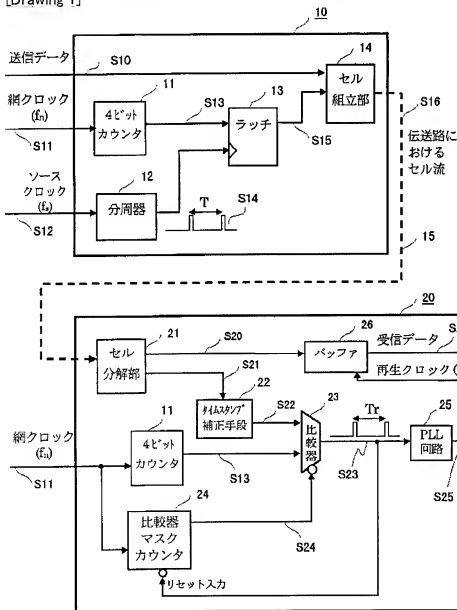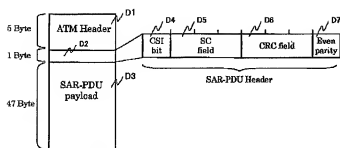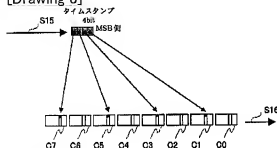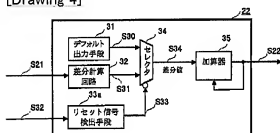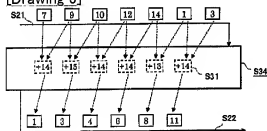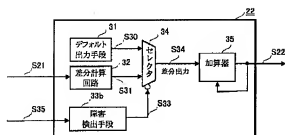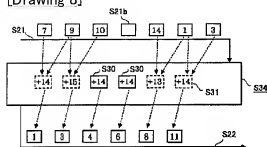
[Drawing 7]

[Drawing 8]

[Drawing 9]
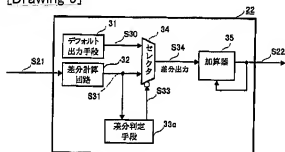
[Drawing 11]
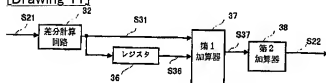
[Drawing 10]

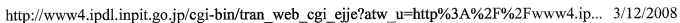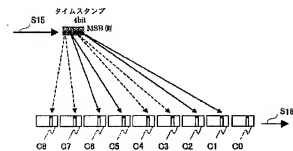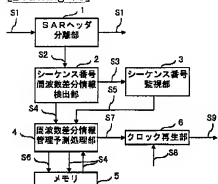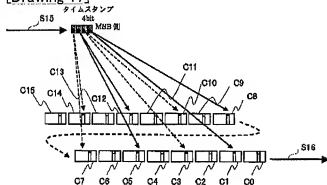[Drawing 12]

[Drawing 13]

[Drawing 14]
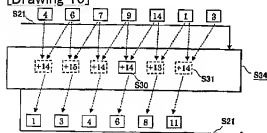
[Drawing 15]

[Drawing 16]

[Drawing 18]

[Drawing 17]

[Translation done.]